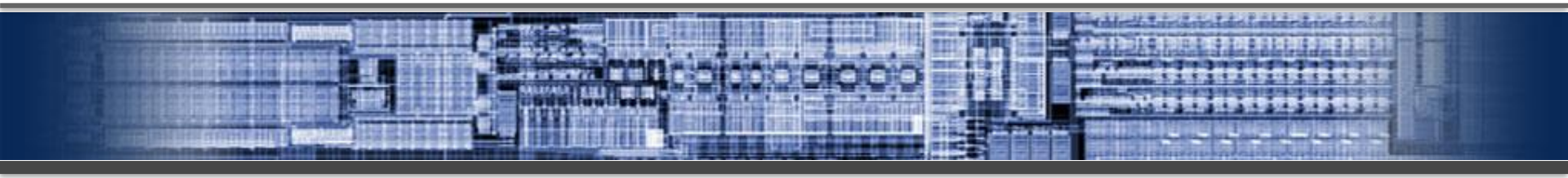


One-size-fits-all PLLs for Advanced Samsung Foundry Processes

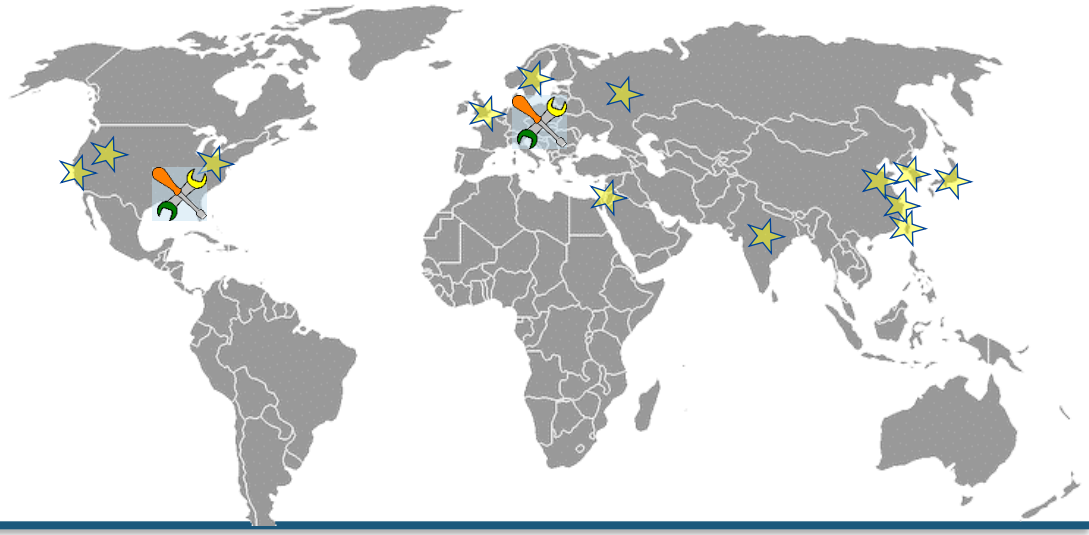
Andrew Cole, VP

Outline

- Silicon Creations introduction
- Kinds of Jitter and a DAC inside a PLL
- Flexible clocking solutions with FRAC PLLs
- Other PLLs
- Summary

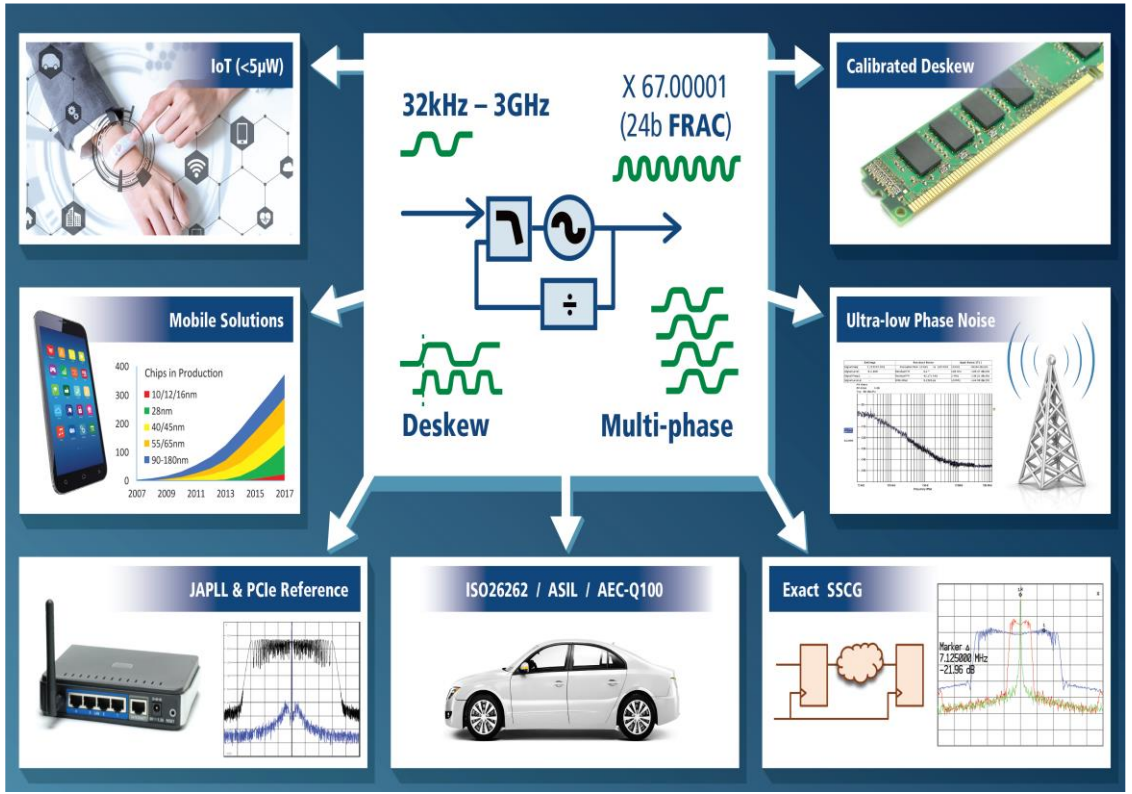
Silicon Creations Overview

- IP provider of PLLs, Oscillators and High-speed Interfaces
- Founded 2006 – self-funded, profitable and growing
- Design offices in Atlanta, USA and Krakow, Poland
- High quality development, award winning support
- >330 customers (>130 in China)
- Mass production in many FinFET process nodes with PLL IPs ready now down to Samsung Foundry 4nm LPE



PLLs from Silicon Creations

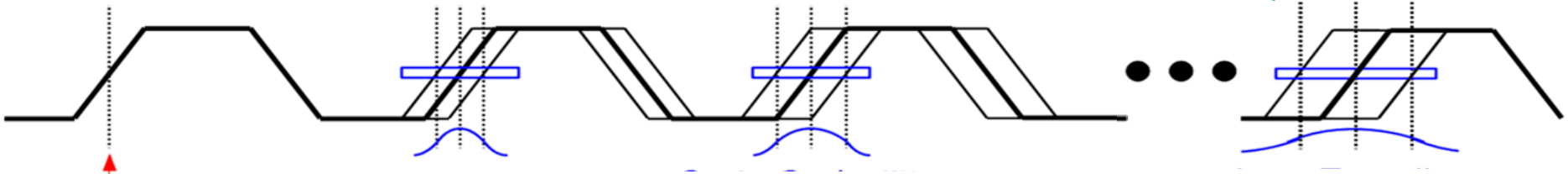
- Highest volume analog IPs
  …
  Our PLLs have been produced on millions of wafers
  …
  robust design and good QA are essential
- PLL products include general purpose, fractional, low jitter AFE, µW IoT, Automotive
- PLLs available now in Samsung Foundry 28FDSOI and FinFET processes from 10LPP/LPE to 4LPE



Outline

- Silicon Creations introduction
- Kinds of Jitter and a DAC inside a PLL
- Flexible clocking solutions with FRAC PLLs
- Other PLLs
- Summary

Types of Jitter



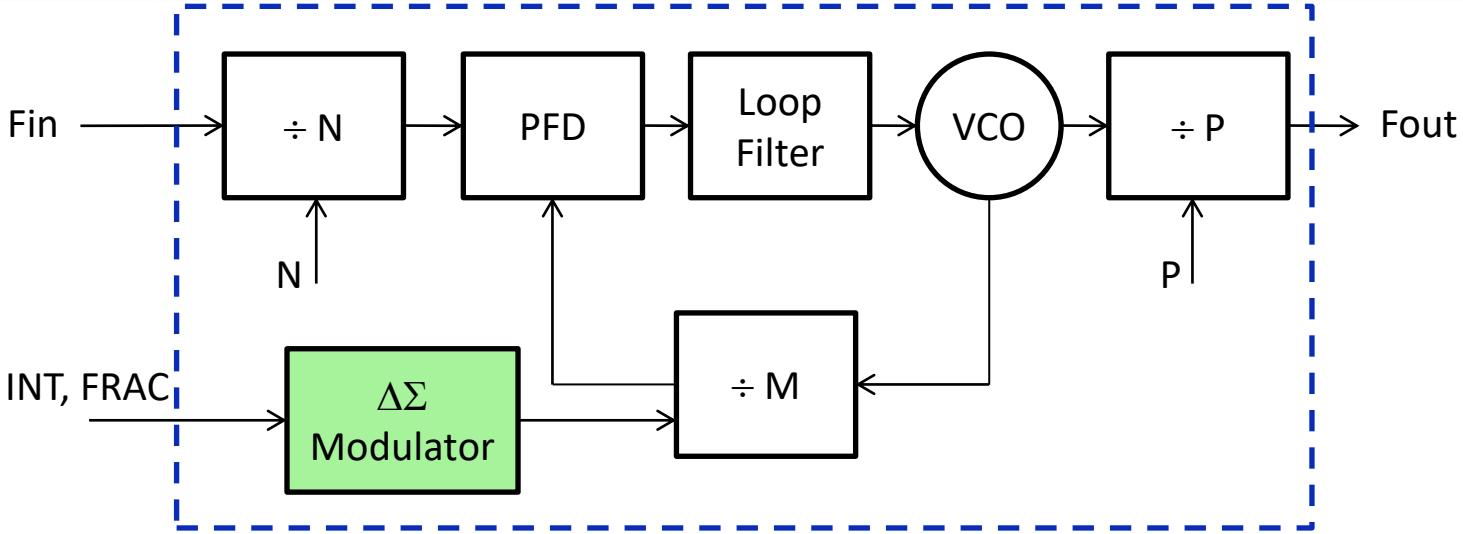
Short term jitter – determined by VCO

Important for digital timing ("STA")

Determined by PLL closed loop

Important for ADC/DAC and SerDes

Fractional-N PLL



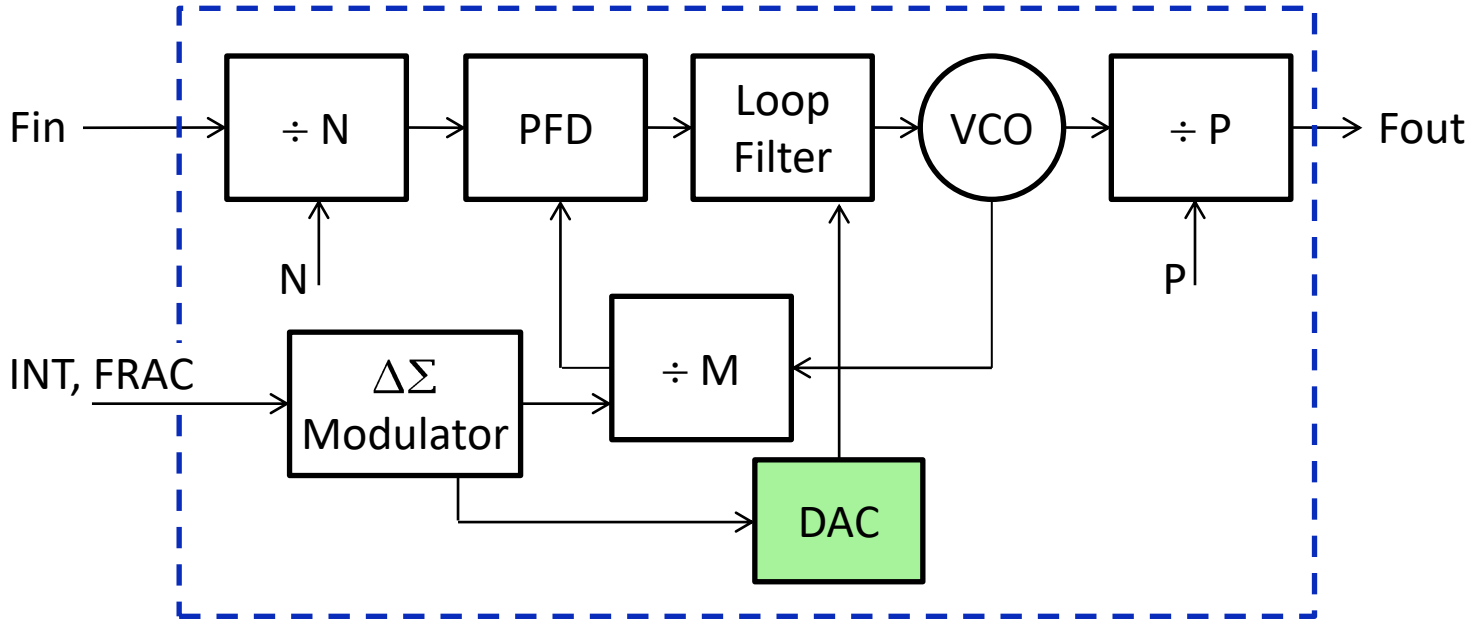
$$M\_avg = INT + \frac{FRAC}{2^X} \qquad Fout = \frac{Fin}{N} \times \frac{M\_avg}{P} \qquad \frac{Fout\_step}{Fout} \approx \frac{1}{M \times 2^X}$$

With $x = 24$ (bits), typical $M > 20$, LSB change in Fout < 0.003ppm (>10,000ppm for integer PLL)

E.g. Average FBDIV of 10.25

"Order"	Values	Sequence
1	10+ 0, 1	0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 1 ☺ Simple ☹ Repeats at ¼ Fin … "spurs" in Fout
3 ✓	10+ -2, -1, 0, 1, 2, 3	1 0 1 -2 3 -2 2 0 0 2 -1 0 1 0 0 -2 1 0 0 1 ☺ Tones (spurs) much reduced ☹ More complex

DAC to Fix Fractional Jitter

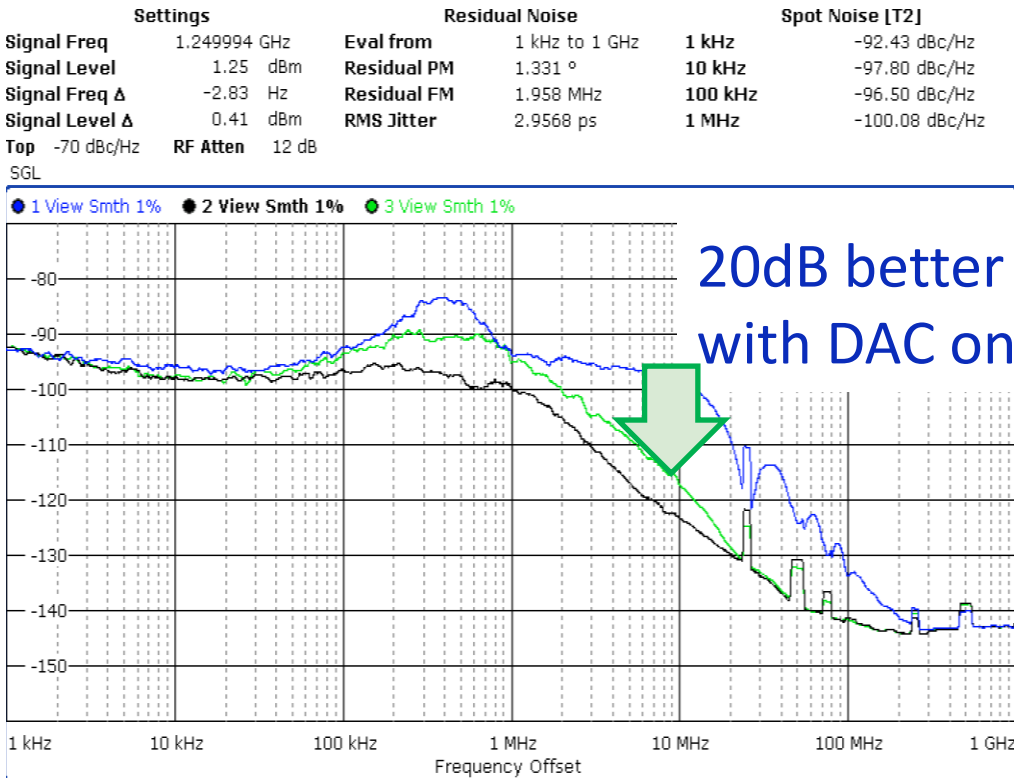


Feed inverse of impulse errors forward to loop filter. DAC re-uses existing transistors and current, so adds almost no area, and almost no power.

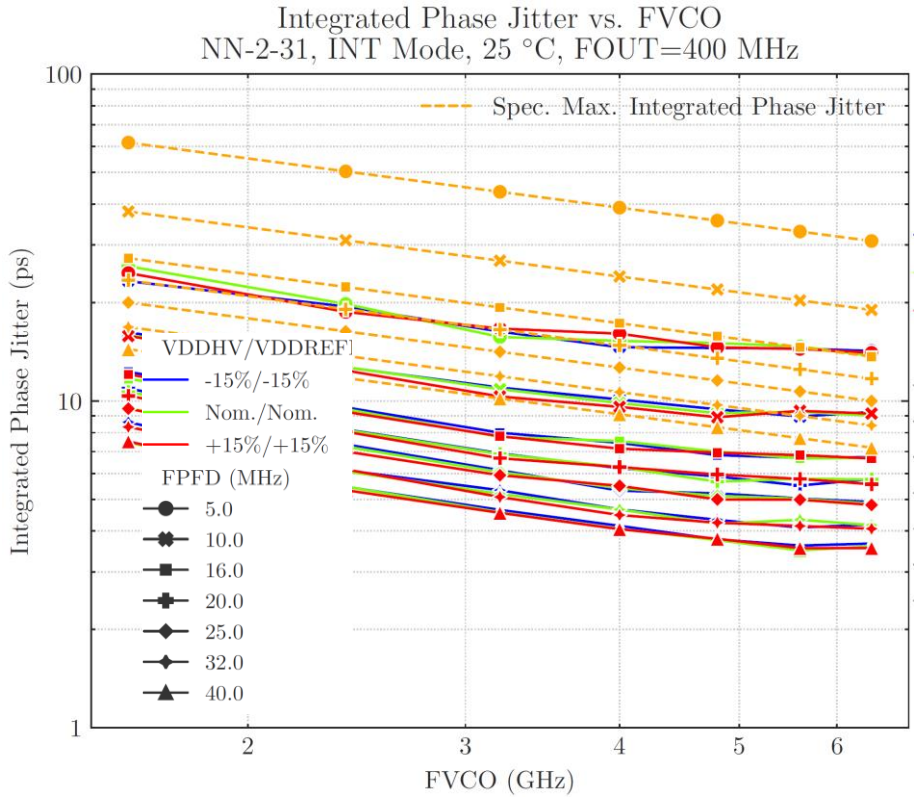
DAC Performance Measured

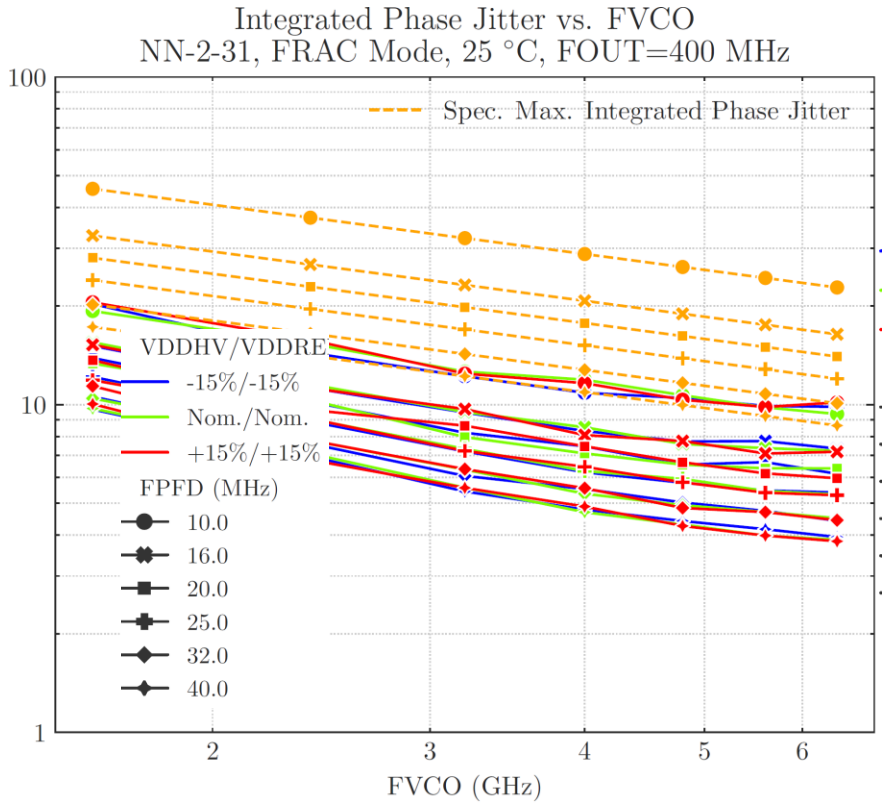
Phase noise with and without DAC. Performance is improved dramatically.

- ✓ Flexible: Any output frequency with any Xtal
- ✓ Good PPA: Use FRAC PLL to make a low jitter clock e.g. SRIS clock for PCIe

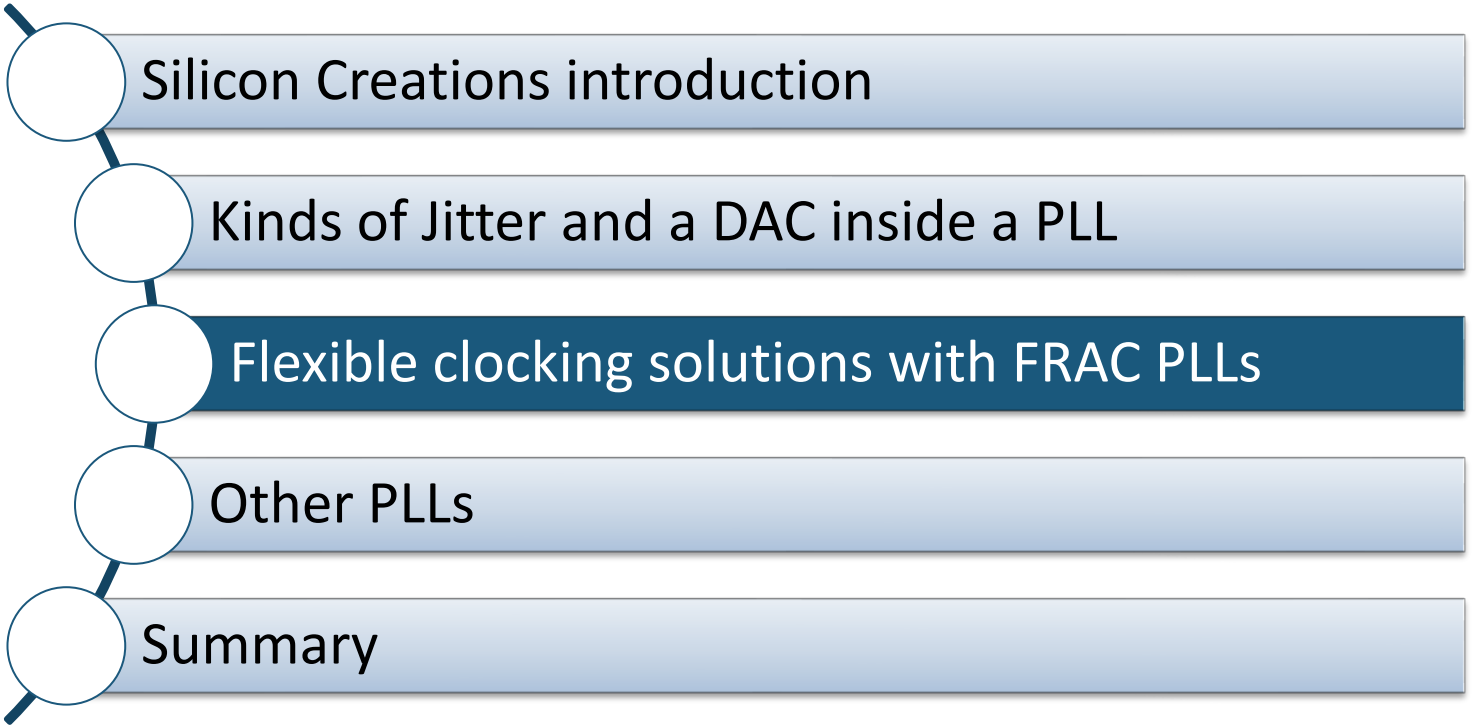


Measurement – SS5LPe

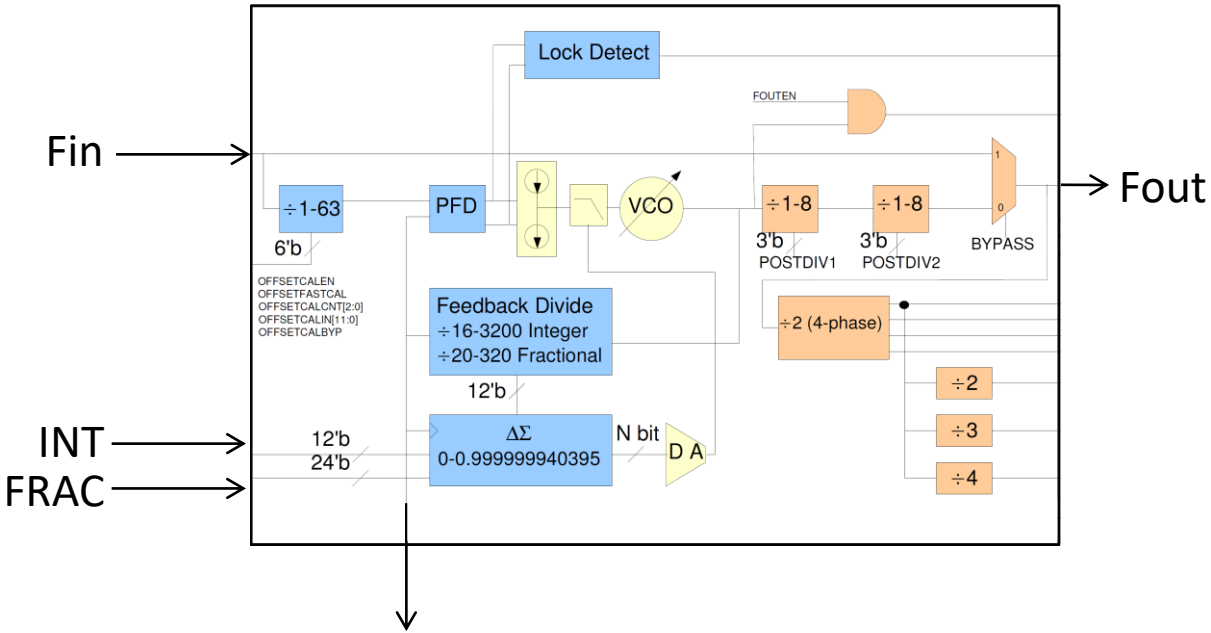




Outline


Silicon Creations introduction
Kinds of Jitter and a DAC inside a PLL
Flexible clocking solutions with FRAC PLLs
Other PLLs
Summary

DFS & Supply Sharing



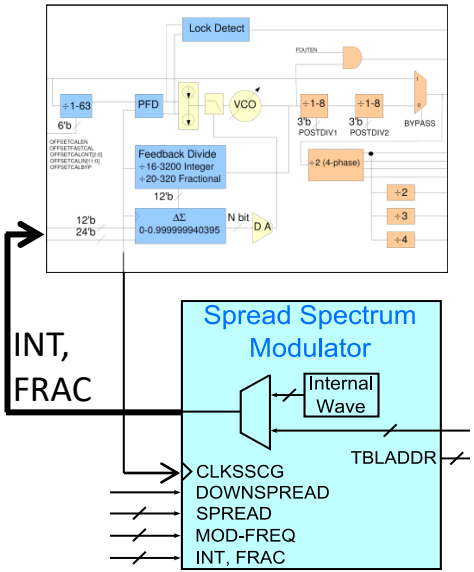
Share supplies with many PLLs for low die area:

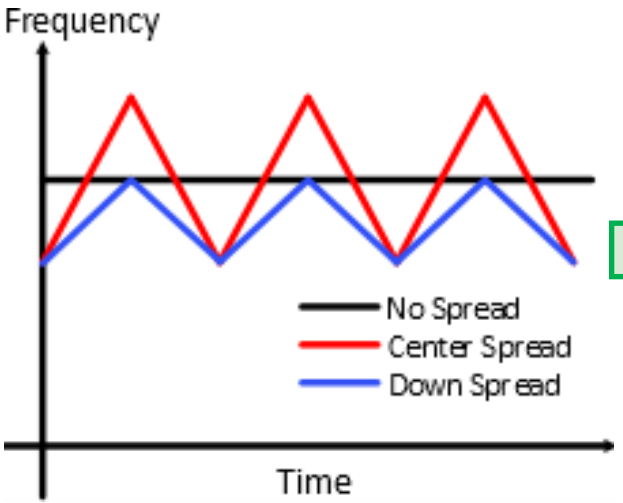
- IO Supply (→ good PSRR)
- Core supplies

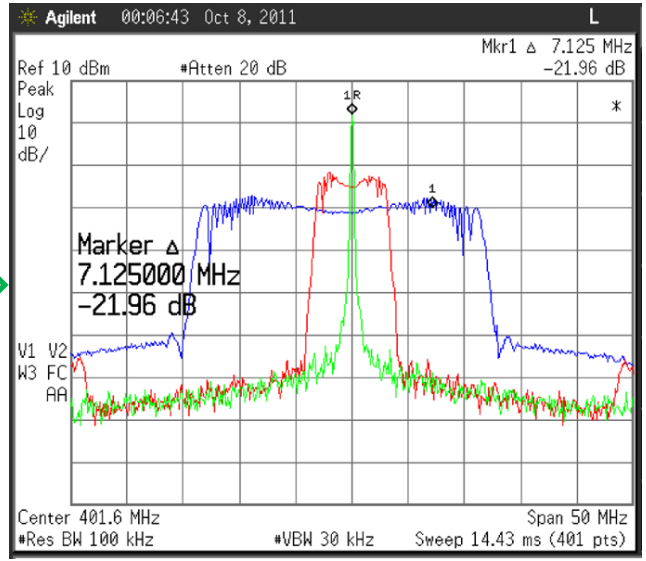
FB Clock output – allows new INT, FRAC on every divided Fin edge. PLL will move predictably to new programmed frequency without losing LOCK for Dynamic Frequency Scaling (DFS).

Exact Spread Spectrum

Digital modulator continuously changes the target frequency for exact spread spectrum shape & modulation frequency. Soft IP (RTL), 4k gates

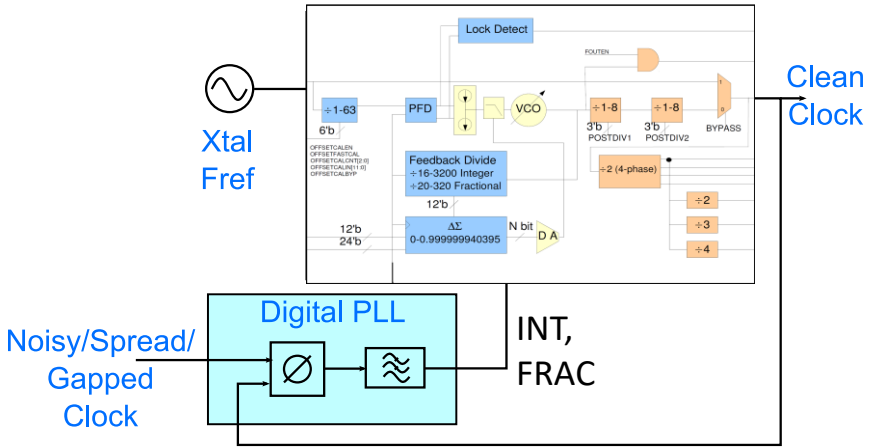


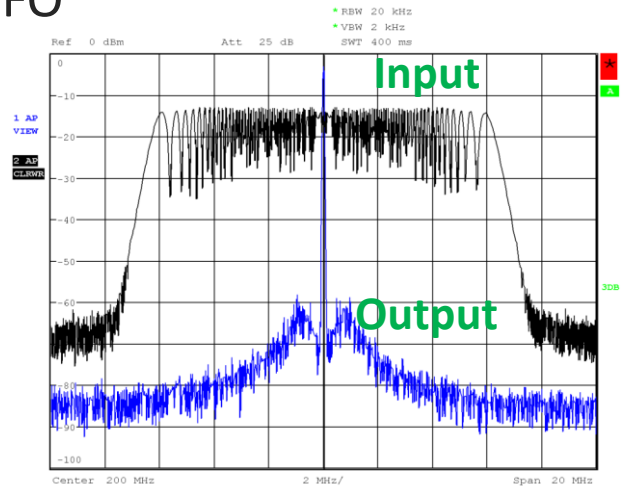




Jitter Cleaner PLL

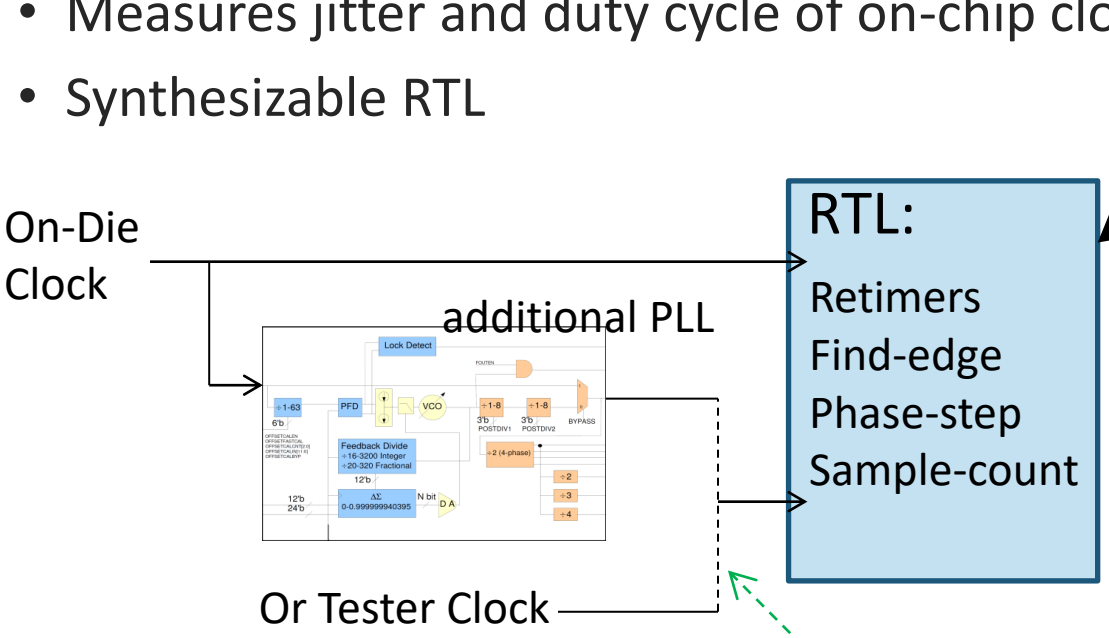
- Digital Filter (RTL ≈19k gates) sets multiplier for fixed clock for FRAC PLL
- Integrated LTJ <1ps and Bandwidth <1Hz possible … replaces $8 to $30 external chip
- Cleans jitter in noisy recovered clock for Sync-E or Optical Networking; Generates average of spread spectrum input for FIFO

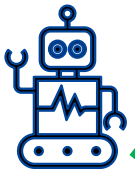




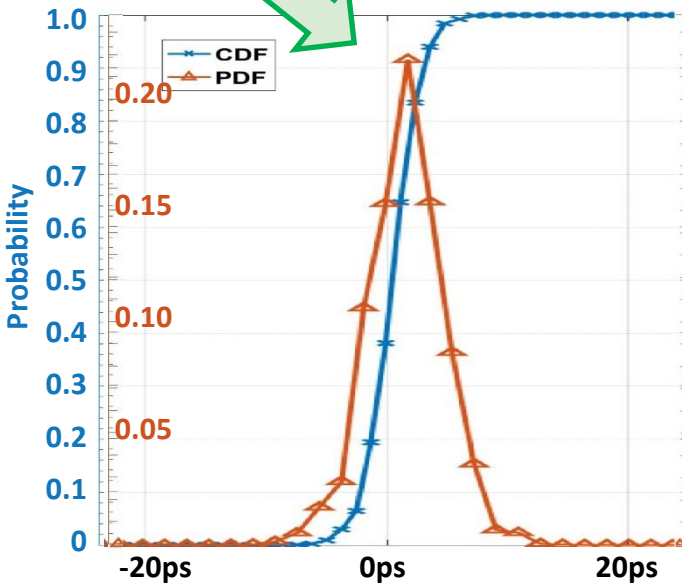
Jitter Monitor

- Measures jitter and duty cycle of on-chip clock
- Synthesizable RTL





Software
(Embedded or Tester)



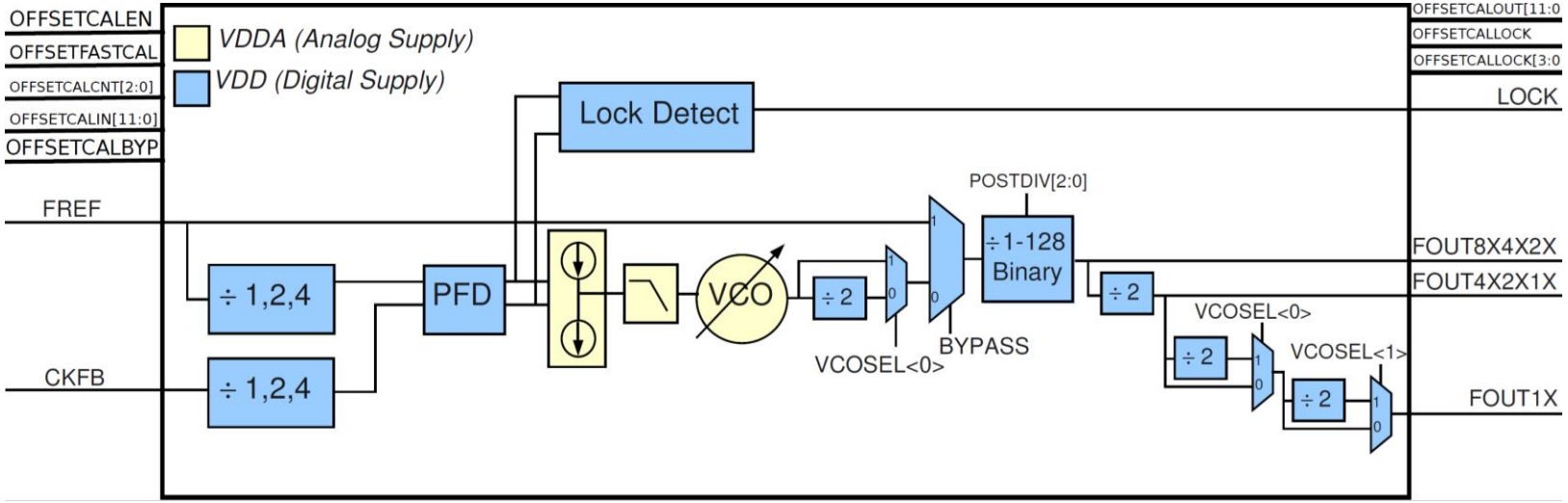
Spare FRAC PLL enables chip to test itself
Or Production Test mode

Outline

- Silicon Creations introduction
- Kinds of Jitter and a DAC inside a PLL
- Flexible clocking solutions with FRAC PLLs
- Other PLLs
- Summary

Deskew PLLs

- Core voltage only: easy to integrate and low power
- Below 0.01mm^2
- Self-calibration of device mismatch



Outline

- Silicon Creations introduction
- Kinds of Jitter and a DAC inside a PLL
- Flexible clocking solutions with FRAC PLLs
- Other PLLs and clocks
- Summary

Summary

- Silicon Creations has been providing reliable, high-performance clocking and SerDes solutions since 2006
- Our Fractional-N PLL is production proven with the highest volumes of any mixed signal IP; Collaboration with Samsung Foundry has helped us provide silicon proven FRAC PLLs in 28FDSOI, 10LPP/LPE, 7LPP, and 5LPP with 4LPE silicon expected soon
- Fractional-N PLLs together with RTL provide very flexible solutions to complex problems with low risk while reducing system BOM or reducing test cost
- For more information, please contact sales@siliconcr.com or visit our booth #1338 on the ground floor

Thank you!

Questions?

For more information:
Visit our Booth (#1338, ground floor)
Contact us: sales@siliconcr.com