Agenda

• Introduction to Silicon Creations and product lines
• The Alphabet soup of Automotive Safety – a brief introduction
• Some of the key deliverables for IP used in Automotive Applications with Safety concerns
• How do we know the PLL is working and safe?
• Showing sufficient reliability for automotive products ... design validation and AEC-Q100 prequalification
Silicon Creations company

- Growing strongly since 2006
- Development in Atlanta & Krakow
- Many products in production from 180nm to 10nm; 7nm proven
  > 350 MP chips
  > 180 PLLs & > 25 SerDes PMAs
- Targeting diverse segments
  - Consumer; Networking; IoT; Automotive; Aerospace; Industrial
- Awarded quality and leading support make us the low risk choice
PLLs from Silicon Creations

Highest volume analog IPs – robust design and good QA are essential e.g.

- TSMC 28nm FRAC PLL
  >105 MP tapeouts, >650k wafers, >1B PLLs
- TSMC 16FFC LAINT PLL
  >5 MP tapeouts, >175k wafers, >2B PLLs

PLL products include general purpose, fractional, low jitter AFE, μW IoT, Automotive
SerDes from Silicon Creations

- Robust and proven from 28nm to 180nm and from <100Mbps to >20Gbps
- Multiprotocol (for FPGA) and targeted protocols
  - SGMII, XAUI, RapidIO, V-by-1 HS/US, FastLVDS, CameraLink, FPDLInk, OIF-CEI, JESD204, CPRI, PCIe1-3, 10G-KR, ...
Automotive Safety at ...

- Silicon Creations engineers have been certified by SGS-TÜV for ISO26262 semiconductor development ... can self-certify IP to ASIL-B
- Have developed and supplied “automotive packages” for IPs including
  - Safety Manual & FMEDEA
  - Design margin & Design reliability reports
- Remainder of talk explains these documents with some examples from our FinFet developments

👍 Does not replace standards, and we can’t guarantee it. Hope to demystify the thousands of pages of documents that help ensure the electronics that drive our cars are safe.

☞ No foundry secrets are disclosed in this presentation, and its not really specifically about 7nm.

👍 No animals were harmed in the creation of this presentation.
“Automotive” Alphabet Soup

• **ISO26262** = a quality standard. Defines procedures and documentation to ensure electronics and products used in cars are safe.
  
  – “**ASIL**” = Automotive Safety Integrity Level
  – How safe – depends on the risk, and effect … “**FMEDA**” and documented in the “**Safety Manual**”

• **AEC-Q100**
  
  – Reliability tests for whole chip: 2,700 parts from 3 wafer lots... no “IP” version defined
  – “**Grade**” = operating ambient temperature range for the (enclosure of the) equipment ... customer needs to translate this to a “**Mission Profile**” for die temperature

... More alphabet soup coming ...
ISO26262 Automotive Safety

- Formally prove that the risk of undetected failure is greater than the lifespan of the system
- ASIL – **Automotive Safety Integrity Level** is a rating for Electrical Systems that govern measures to ensure safety based in consequences of failure

<table>
<thead>
<tr>
<th>ASIL</th>
<th>Safety consequences of faults for end users...</th>
<th>IP Vendor needs to:</th>
</tr>
</thead>
<tbody>
<tr>
<td>-A</td>
<td>Equipment damage possible, inconvenience</td>
<td>Make good IP</td>
</tr>
<tr>
<td>-B</td>
<td>Injury possible</td>
<td>Document carefully &amp; <strong>self certify</strong>; IP might need AEC-Q100 testing</td>
</tr>
<tr>
<td>-C</td>
<td>Injury is likely</td>
<td>Convince <strong>Independent Auditor</strong> documents are good; IP might need AEC-Q100 testing</td>
</tr>
<tr>
<td>-D</td>
<td>Serious injury, very likely, death possible</td>
<td>?</td>
</tr>
</tbody>
</table>
Key concepts: SEooC & FTTI

- **SEooC** = “Safety Element out of Context” is an ISO26262 concept that enables component (i.e. IP) developers to independently define the Safety performance of the IP for a UseCase.

- **UseCase** is defined by the **FTTI** (Fault Time Tolerance Interval: how quickly the system must respond to a Fault ... the system designer = IP/chip customer determines this)
  - PLL go/no-go testing (e.g. clock still there?) is quick: is on the order of the output rate
  - Performance metrics like DCD and jitter require precise detection mechanisms and averaging – takes longer
  - Transient faults can be nastier, and cause might be unclear (random noise or a transient event – e.g. gamma particle)
  - Not all functions are Safety Critical (e.g. unused outputs, DFM features like scan chains) .. i.e. context is important
A Safety Manual is defined in ISO26262 provides the System Safety Engineer (customer) our understanding of how to monitor our IP and determine the risk of failure of the IP

- Safety Goals – inability to maintain performance or timing is considered a Safety Violation:
  - What is the IP supposed to do?
  - What might constitute an IP failure?
  - Datasheet Performance Specifications & Timing Requirements in Liberty models

- Define UseCases
  - Guidance for detecting IP failure (diagnostics internal and external to the IP)

- Inputs for the FIT (Failure In Time = failure rate) for the IP with assumptions/definitions allowing calculation of FIT in the system
PLL External Diagnostics

- External diagnostics designed to detect faults in clocks for UseCases
- Counters can detect frequency errors, cycle slips, stopped clocks (small errors take longer to detect)
- Two fractional PLLs can measure each other ... \( \Delta \text{Freq.} = \Delta \Phi / t \) ... Phase difference, duty cycle, or even jitter (Tessent® PLLTest from Mentor)
== Failure Mode Effect and Diagnostics Analysis (defined in ISO26262)

- Analysis method that enables the SEooC development and documents the expected failure rate of the IP for key specifications and timing
- Tied to Safety Manual via Safety Goals and Violations
- Failure modes derived from
  - Failure of internal block outputs (for each internal block output how could failure impact a datasheet parameter?)
  - ISO2626 recommends failures appropriate to many IP components
- Customer can remove failures that do not constitute a Safety Violation in their system from the FMEDA. E.g. Failure of a particular output or block might not cause the IP to violate their Safety Goal
- Note: FMEDA ≠ DFMEA
Making the FMEDA

<table>
<thead>
<tr>
<th>Block Name</th>
<th>Component/type</th>
<th>Failure modes (delete if don't matter)</th>
<th>Calc FIT for block</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lock Counter</td>
<td>N, M, A = xxx</td>
<td>x, y, z, t</td>
<td>0.001</td>
</tr>
<tr>
<td>POSTDIV</td>
<td>N, M, A = xxx</td>
<td>x, y, z, t</td>
<td>0.001</td>
</tr>
<tr>
<td>DSM</td>
<td>N, M, A = xxx</td>
<td>x, y, z, t</td>
<td>0.001</td>
</tr>
<tr>
<td>REFDIV</td>
<td>N, M, A = xxx</td>
<td>x, y, z, t</td>
<td>0.001</td>
</tr>
<tr>
<td>FBDIV</td>
<td>N, M, A = xxx</td>
<td>x, y, z, t</td>
<td>0.001</td>
</tr>
<tr>
<td>VCO</td>
<td>N, M, A = xxx</td>
<td>x, y, z, t</td>
<td>0.001</td>
</tr>
<tr>
<td>QPMP</td>
<td>N, M, A = xxx</td>
<td>x, y, z, t</td>
<td>0.001</td>
</tr>
<tr>
<td>Startup</td>
<td>N, M, A = xxx</td>
<td>x, y, z, t</td>
<td>0.001</td>
</tr>
<tr>
<td>FPFD</td>
<td>N, M, A = xxx</td>
<td>x, y, z, t</td>
<td>0.001</td>
</tr>
<tr>
<td>Loop Filter</td>
<td>N, M, A = xxx</td>
<td>x, y, z, t</td>
<td>0.001</td>
</tr>
<tr>
<td>Top</td>
<td>N, M, A = xxx</td>
<td>x, y, z, t</td>
<td>0.001</td>
</tr>
</tbody>
</table>

Equipment ambient stress → Packaging → FIT Rates for circuit based failure modes

FIT in equipment = ∑ Block FIT rates scaled by factors for type of fault & diagnostics. ...
... only for failures that matter (i.e. violate a safety goal)

Chip/system designers  →  IP/component designers

Automotive Safety - Reuse 2017
In reality

- Simplification of previous page is Andrew’s doing and causes Safety experts to cringe. Reality is nowhere near as simple:

- Detailed FIT numbers & calculations used by system designers to roll up to failure rates for their chip:
DFMEA

== Design Failure Mode and Effect Analysis

- Structured design analysis: Brainstorm to consider what can go wrong with the IP and prioritize issues for fixing and testing
- For each failure mode, assign qualitative levels to
  - X = likelihood failure will occur in the design
  - Y = how serious the impact of the failure is
  - Z = how easily we can know it has happened

Sort by composite score
\[
= (X \times Y \times Z)
\]

- Useful to focus effort on production test and IP evaluation
- Along with a formal design review this can supplement the FMEDA and increase customer confidence
Reliability – Grades

• “Automotive Grade” in AEC-Q100 defines the ambient temperature range for the end equipment
  – Grade ...0 = -40°C to 150°C; ...1 = -40°C to 125°C; ...2 = -40°C to 105°C
  – Scary! But most equipment has a “Mission Profile”

• Translated by equipment designers to a Mission Profile for the chips (and IP):
  – E.g. “Worst case Grade 0 die temperature in our product = 25 yrs with 20% @ ≤65°C; 40% @ 95°C; 30% @ 125°C; 10% @ 150°C”

• IP designer translates this to an equivalent number of hours at one (high) temperature for electromigration reliability design and verification ($TTF = A.J^{-n}.E^{Ea/kT}$)
  – Results far less scary for EM than 25 yrs @ 150°C
Reliability – Failures

Transistors fail due to electrical stress:
- **GOI** = Gate-Oxide Integrity
- **HCI** = Hot Carrier Injection
- **NBTI** = Negative Bias Temperature Instability
- **TDDB** = Time Dependent Dielectric Breakdown

**Goal:** Cumulative failures allowed (e.g. 0.1%)

**Design stats:**
- Total gate area used
- Gate length used
- % operation AC/DC
- Max operation voltages
- Tj max (assume WC)

**Lifetimes for GOI, HCI, NBTI & TDDB**

**Tools from foundry (process dependent)**

Lifetime meets goal (report)

Lifetime does not meet goal

→ Fix design

WC... usually not a Mission Profile
Reliability – Aging

- Circuits change because component characteristics change over life due to stress
- In Fin Fet transistor (local) self heating changes behavior and accelerates change
- Spice can predict issues with IP due to device aging

Simulate @ WC stress condition

Make Spice models for degradation
  \[ f(\text{lifetime, self-heating}) \]
  (method foundry dependent)

Compare key parameters
Reliability – Aging example

Example for 7nm IoT PLL

– WC stress = SS corner, 10 years, 125°C, Vdd’s +10%

<table>
<thead>
<tr>
<th></th>
<th>Before</th>
<th>After</th>
<th>Δ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current consumption</td>
<td>41.8uA</td>
<td>42.9uA</td>
<td>2.6%</td>
</tr>
<tr>
<td>FOUTVCO frequency (open loop)</td>
<td>99.3MHz</td>
<td>94.6MHz</td>
<td>-4.7%</td>
</tr>
<tr>
<td>FOUTVCO Duty Cycle</td>
<td>49.4%</td>
<td>49.4%</td>
<td>-0.08%</td>
</tr>
</tbody>
</table>

→ Conclusion: drift of characteristics is minimal, performance will remain well within specification.
**AEC-Q100 Prequalification**

- End-product qual. uses >2700 parts from 3 wafer lots
- Customers won’t pay for this for most IPs
- “Pre-qualification” protocol agreed with a key customer → Minimize risk of missing the market window when end-product fails qual.
- <100 parts from two MPW wafers

**Details (read them later):**

1. **Screen test** with tracked part numbers to allow post mortem (Room temp, one supply voltage, functionally OK, record key performance parameter(s), leakage and operating power supply currents)
2. **ELFR** = 80 parts; 48 hrs @ 125°C, supplies at 120% (or max allowed by foundry), max operational stress
3. **Screen Test** (PASS = off/static current <50% larger, supply current <10% larger, key performance < 10% worse)
4. **HTOL** = 77 parts (all the passed parts from ELFR test), 1,000hrs @ same conditions as ELFR
5. **Screen Test** (same test PASS criteria from before ELFR; parts failing ELFR or HTOL need to be debugged, and failure explained if in Silicon Creations IP)
6. **ESD** = For each of HBM (2kV only), MM (200V only) and CDM (500V / 6A only), stress 3 parts each supply pin connected to IP under test (3 parts for each supply)
7. **LUP** = 3 parts: At 125°C, all stressed with typical input/output current for each pin connected to IP ±100mA; 150% of typical supply levels for 10 sec.
8. **Screen Test** & report ESD and LUP parts (same test PASS criteria from before ELFR results; parts failing ESD or LUP need to be debugged, and failure explained if in Silicon Creations IP)
Conclusions

• Silicon Creations has worked on automotive projects or provided automotive documents for PLLs and SerDes in 40nm, 28nm, 16nm and 7nm
• Lots of paper
• No such thing as a “standard automotive package” – contents and cost vary widely by end product and customer QA conventions
• Too many acronyms (three letters not enough!)
  → Need training to understand the docs, let alone make them
• Imposes good design practice and does make IP better