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Architectures and IP for SoC Clocking

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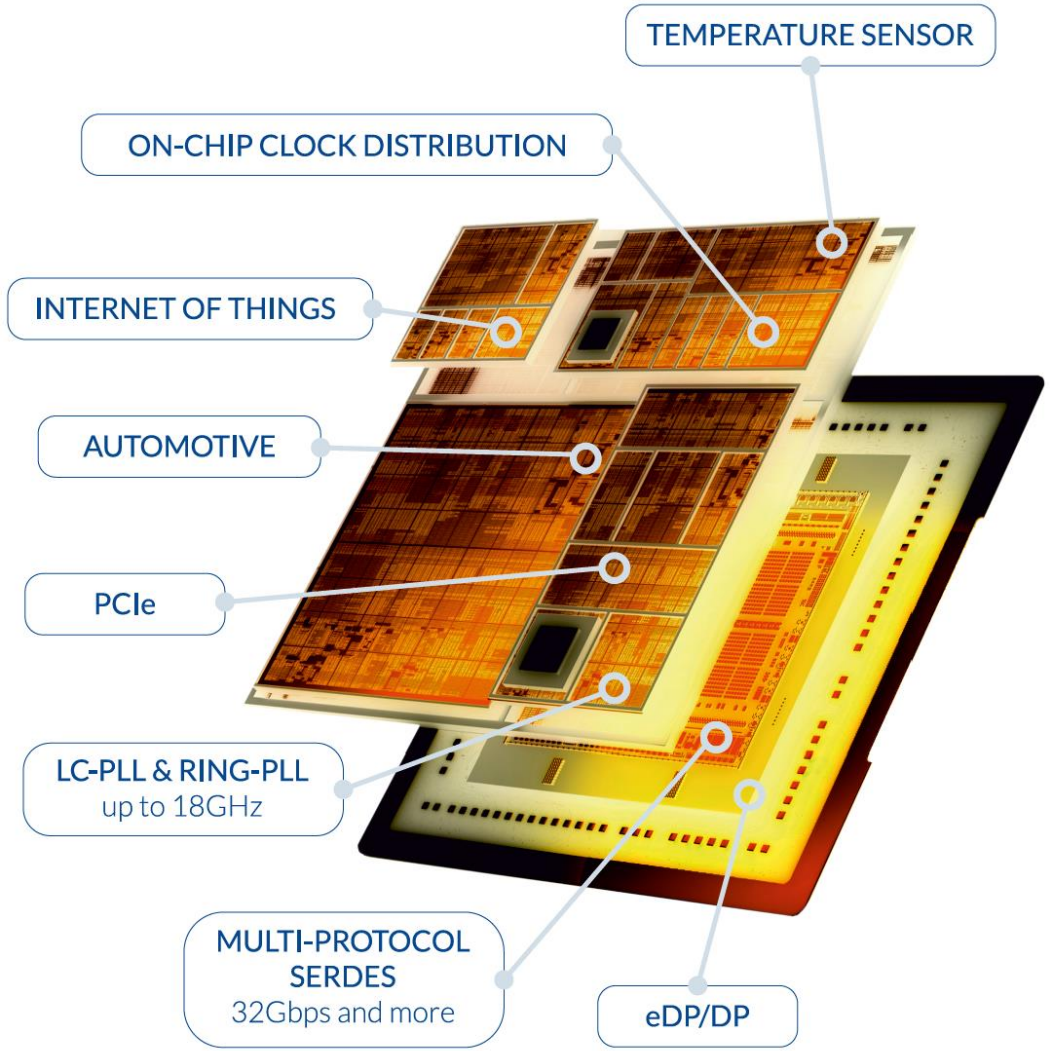


PLLs, Oscillators & High-speed Interfaces

Majority of World's Top 50 IC companies work with us

PLANAR

FD-SOI

GAA

FinFET

Silicon Creations

Silicon Creations in numbers

1500+
Chips using our IP

11M+
12” wafers shipped using our IP

700+
Unique IP products

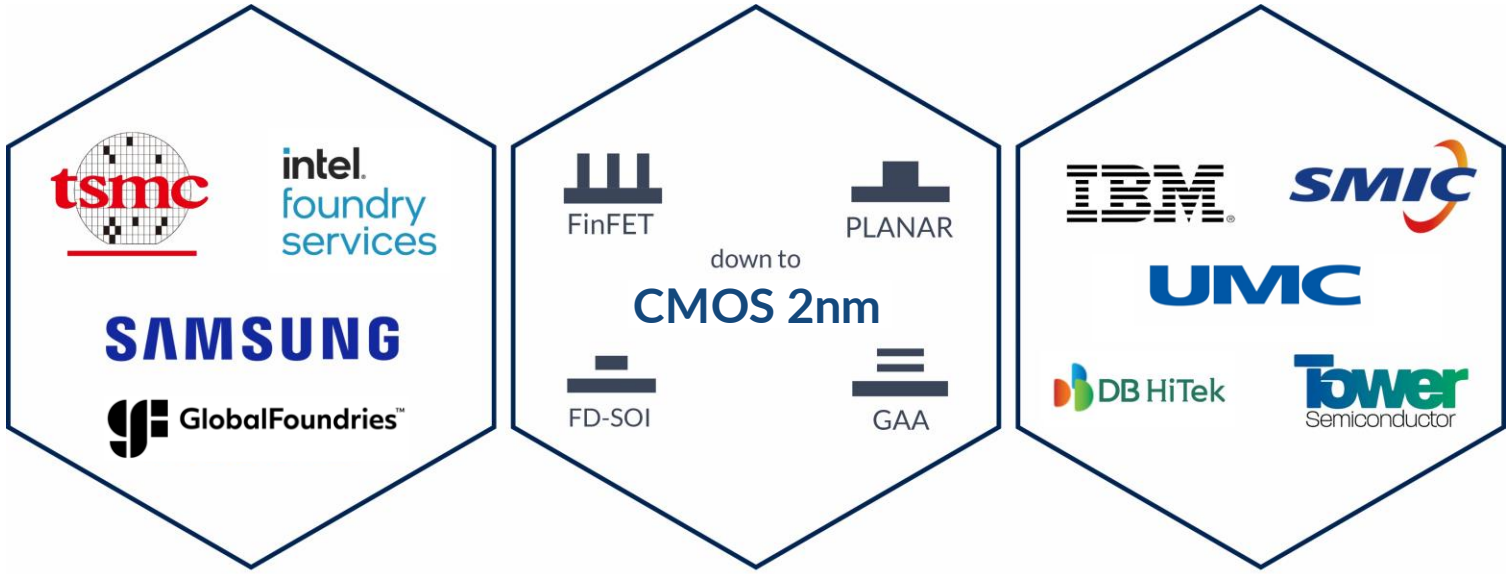
500+
Customers

150+
Production tape-outs annually

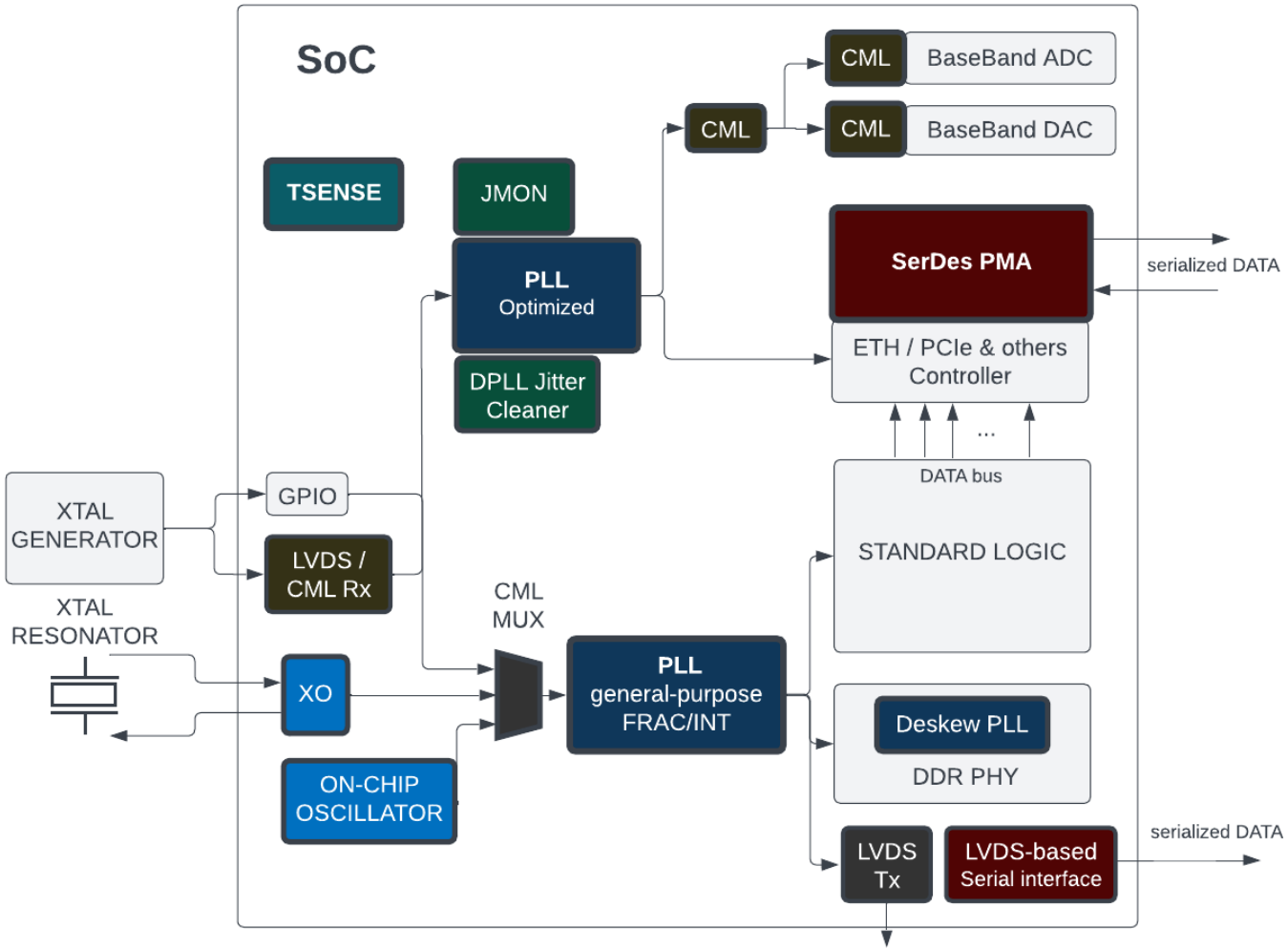
2nm
Available today

ISO 9001 2015 CERTIFIED

Automotive
ISO 26262 ready



Silicon Creations IP in today SOCs



General-Purpose & Specialized **PLLs** **+RTL** upgrades

High-Performance **LVDS I/O**

Multiprotocol **SerDes**

Oscillators & XO

CML cells for On-Chip Signaling

Legend PLL | Clock distribution | RTL IP | Analog IP | Oscillators | SerDes | 3rd party

Optimized Clocking IP Portfolio

General Purpose IP

- INT PLL
- FRAC PLL
- XO 8-40MHz
- OSC 1-24MHz
- DESKEW
- BAND-GAP
- PoR
- TSENSE
- Delay-to-Digital DDC

High-Performance /Specialized PLL

- Frequency Generator FG
- 8/16-PHASE MPINT
- High-BW HBFRAC
- Low-Jitter LJFRAC
- LC-PLL
- Low-Jitter LJINT

Supplementary RTL

- JITTER-CLEANER DPLL
- Spread-Spectrum SSMOD
- Digital Phase Aligner DPA
- Jitter-Monitor JMON
- Frequency Jumper
- LOCK COUNTER

Low-Power /Low-Area PLL

- Low-BW LBINT IoT
- Low-Area LAFRAC
- Low-Area LAINT
- Low-Power LPFRAC

Clock Distribution

- DIVIDER
- CMLMUX
- LVDS Tx/Rx

Automotive

- FMEDA
- SAFETY MANUAL
- DFMEA

Legend

- Analog IP
- PLL
- Documentation
- Clock distribution
- RTL IP
- Oscillators

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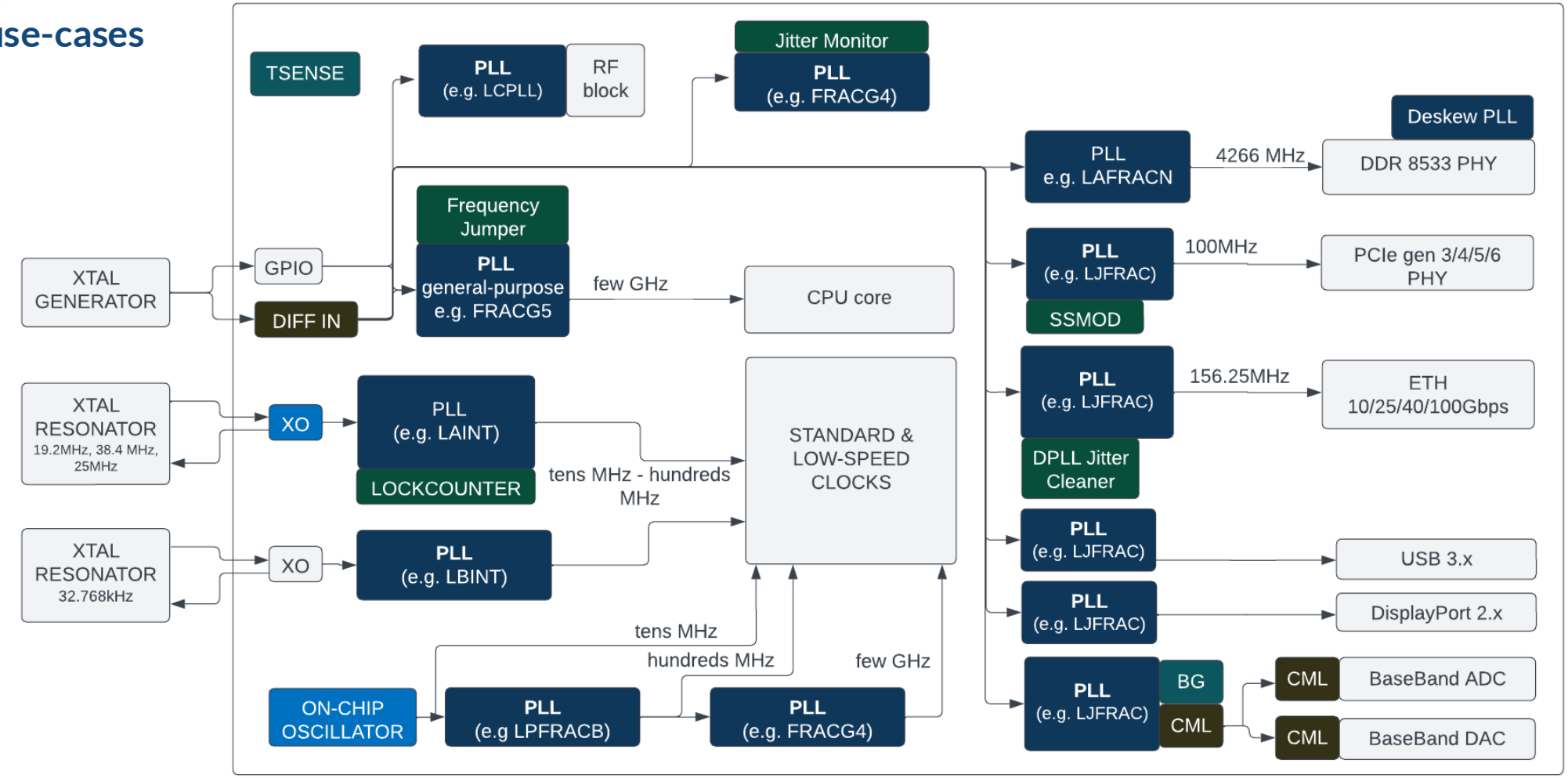
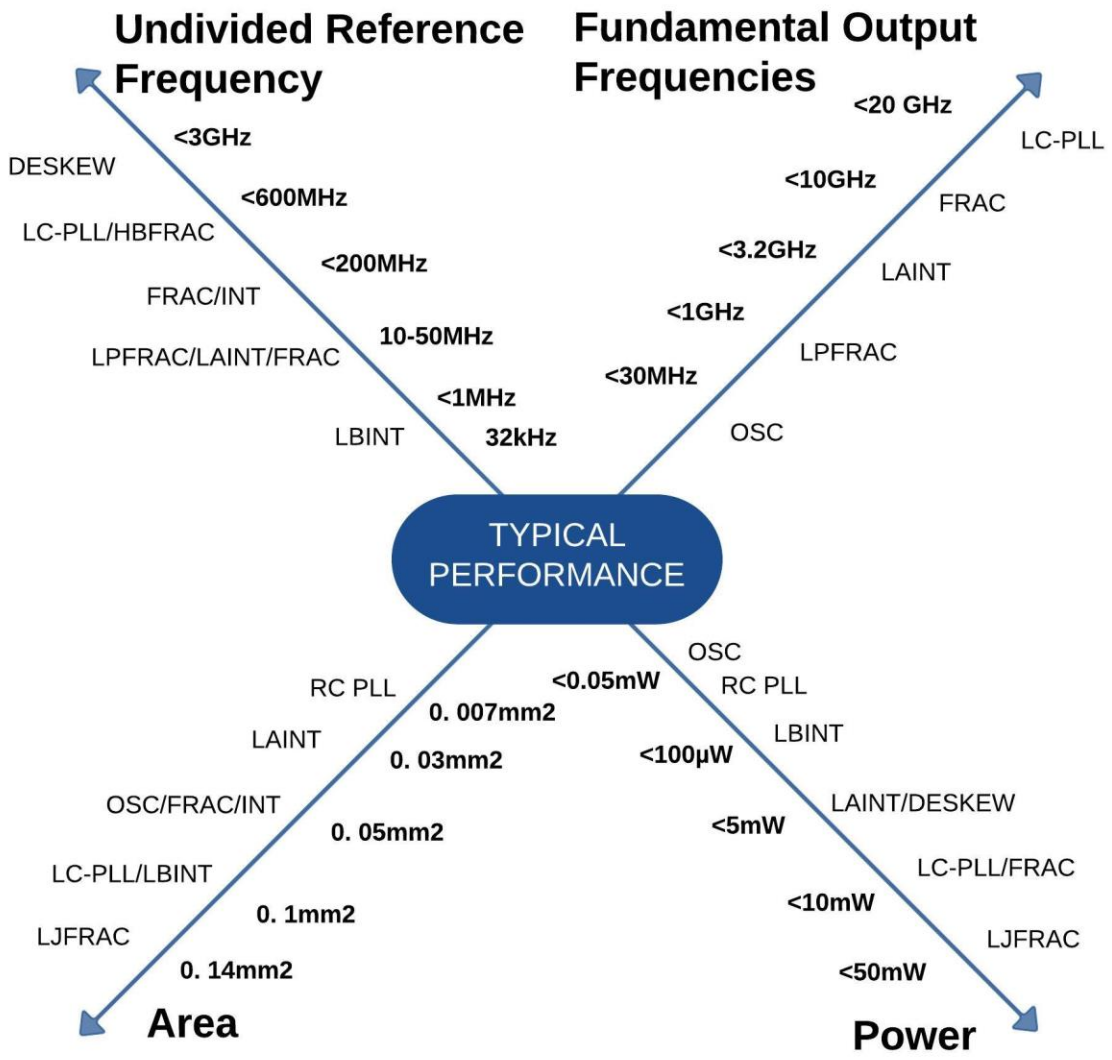
SoC Clocking Options using specialized SiCr IP

Selected use-cases



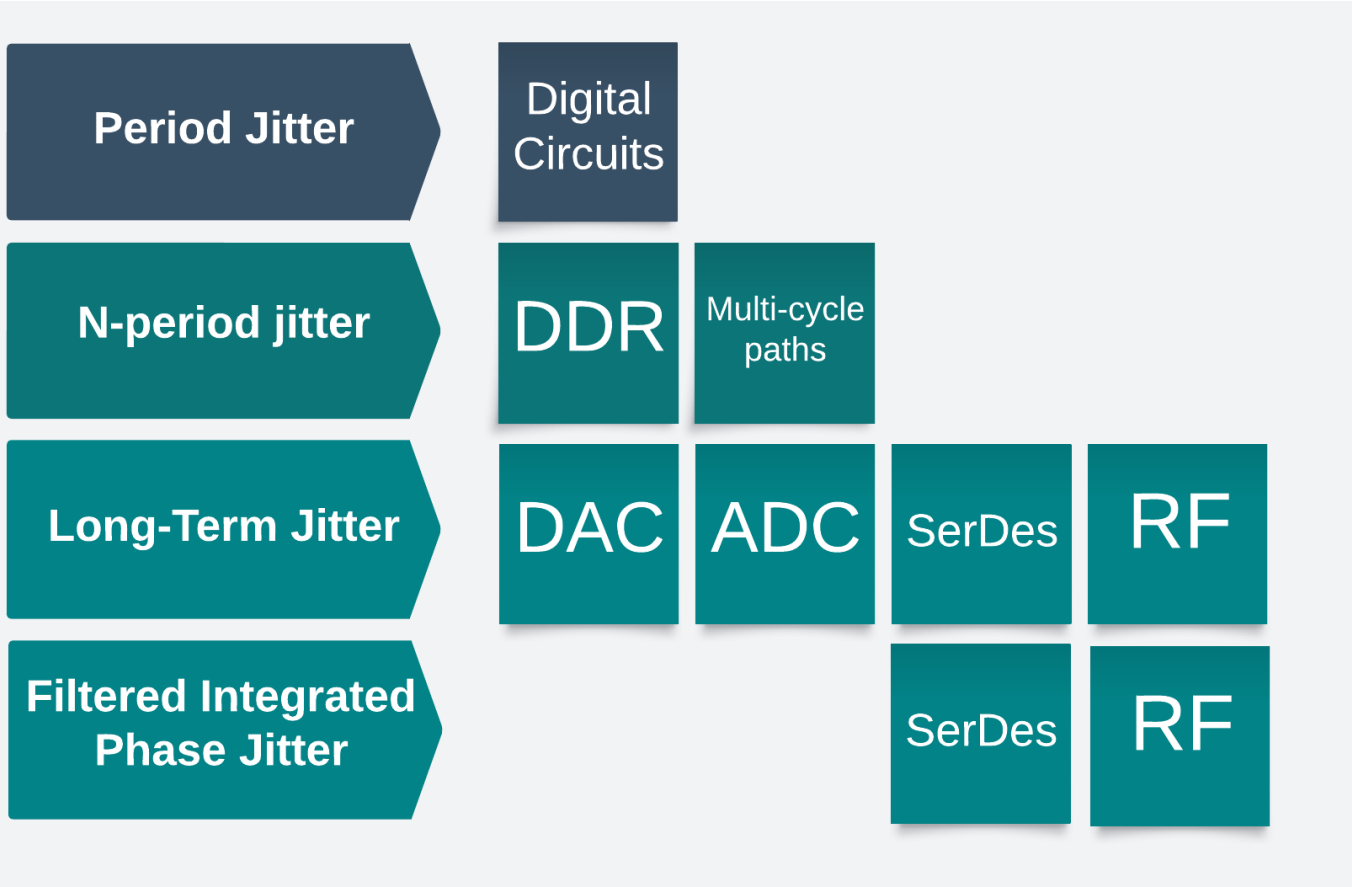
PLL Performance Matrix : Frequency, Area, Power



Silicon Creations PLL IP covers a vast range of performance indicators and can be a fit to many applications.

- **Power:** below 50 µW through 5mW up to 50mW
- **Area:** 0.07mm^2 through 0.1mm^2 up to 0.14mm^2
- **Output Frequency Range:** From MHz range up to tens of GHz; frequency jumping, glitch-free operation, deskewing
- **Reference Frequency Range:** From 32kHz, through all crystal oscillator types, external clock chips, on-chip deskewing.

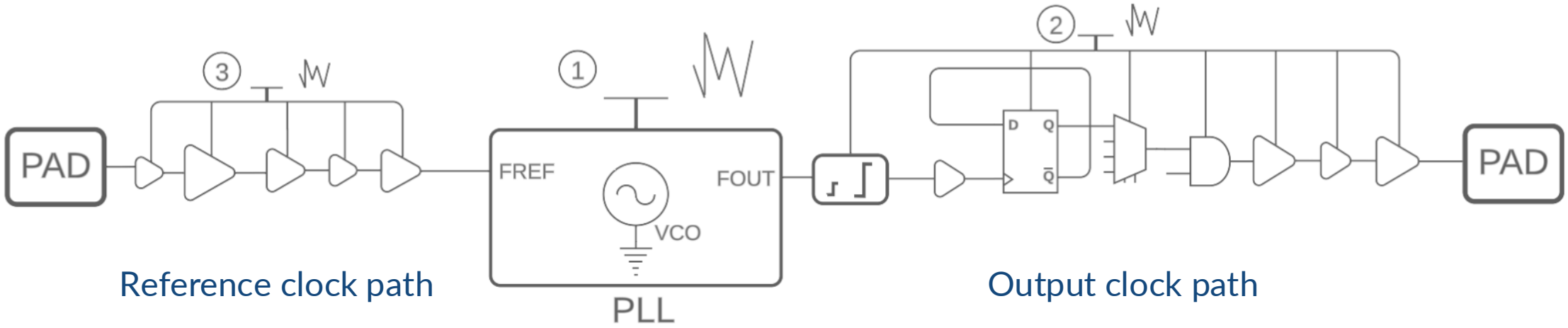
Jitter types by application



Various applications require different clock quality metrics.

- **Generic, digital synchronous logic:** Total period jitter (peak-negative) to define clock uncertainty for STA.
- **Multi-cycle paths and e.g. DDR controllers:** N-period jitter (depending on number of cycles / latency)
- **ADC/DAC:** Long-term jitter / Phase Noise to achieve ENOB; LJT reduces ENOB
- **RF:** Long-term jitter / Phase Noise to low EVM; LTJ rotates constellation increasing EVM
- **SerDes:** Clock Specification (including integration bands) tightly related to the protocol and PHY vendor. Possible filtering (e.g. PCIe spec). Embedded clock applications require low LJT.

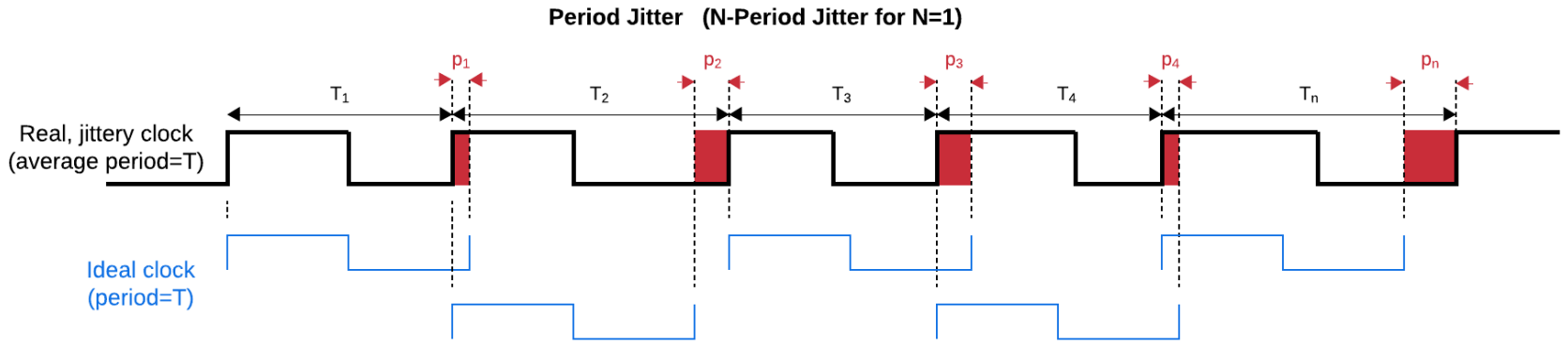
Sources of Jitter

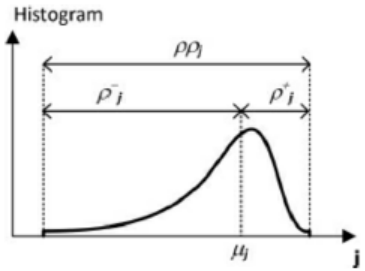


Several factors impact jitter in SoC environments, but their effects vary significantly. Key contributors include:

- FREF signal quality including impact from its signal path -> design choices
- PLL design and operating point (FPFD, FVCO, FOUT configuration, PVT condition) -> IP vendor + Programming
- PLL conditions (decoupling, supply noise) -> IP vendor support + design choices
- Output clock path (supply noise, length / delay, additive jitter) -> design choices

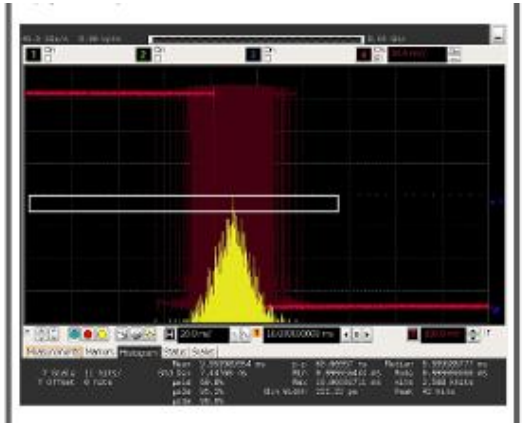
Types of jitter : Period Jitter





TOTAL JITTER (TJ @ BER 1E-12)

expressed in ps peak-to-peak, or peak-negative



$$TJ = DJ_{\delta\delta} + RJ(Q)$$

Random component (RJ @ Q=7)

\+ (arithmetic sum)

Deterministic component (DJ)

Expressed in ps RMS as standard deviation (σ) of Gaussian distribution.
Q=6-8 is often used to bound the worst-case peak-to-peak jitter

Reference-rate Correction

Supply-Noise Induced

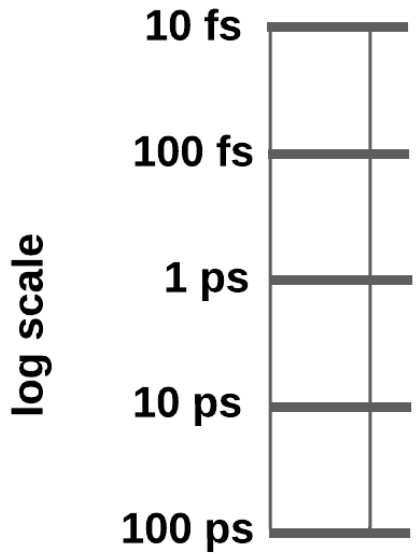
Period Jitter

- Period Jitter is the deviation of each period from the ideal.
- Primary concern for digital clocking
- PJ can be natively measured by oscilloscope
- Peak-to-Peak jitter, or period jitter @ BER, can be estimated by jitter decomposition and using crest factor

Period Jitter & System Contributions

Period Jitter RMS (random)

at equivalent 400MHz carrier
(subject to scaling: the higher FOUT the lower period jitter)



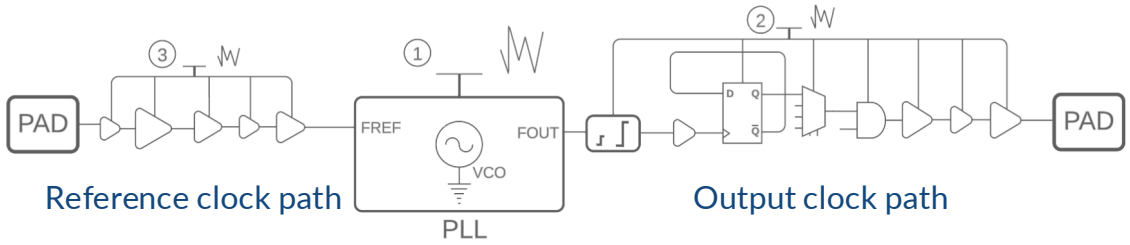
IP Group (exemplary)

LCPLL

LJFRAC

FRAC / INT
DESKEW / LAINT

RC-PLL

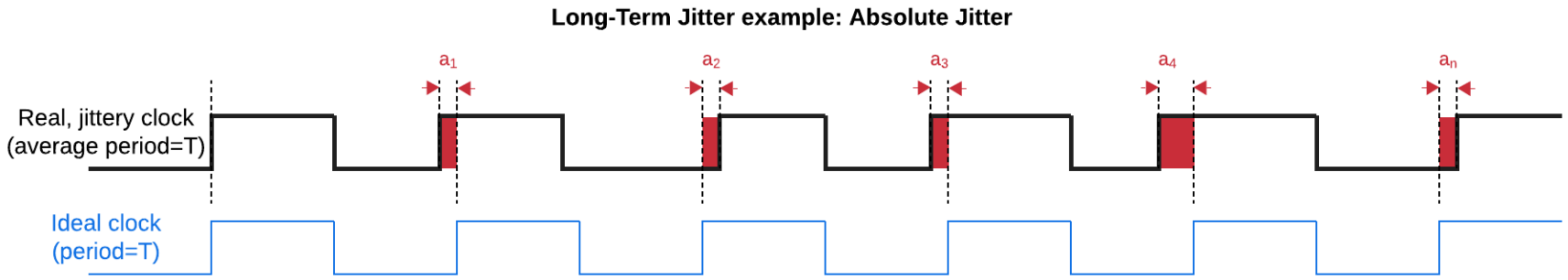


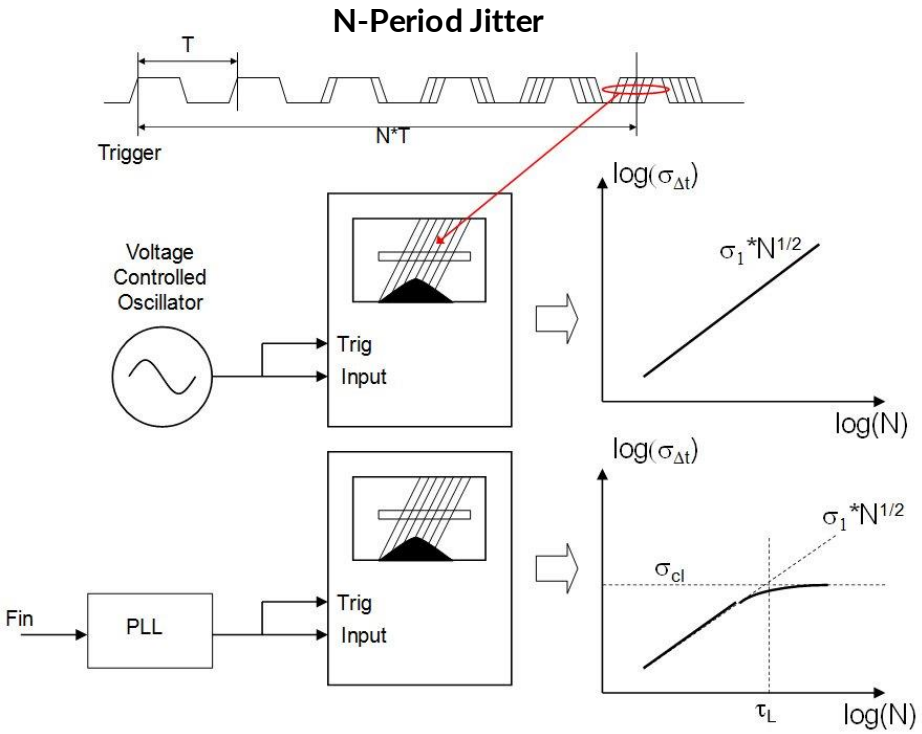
Important design aspects for best performance

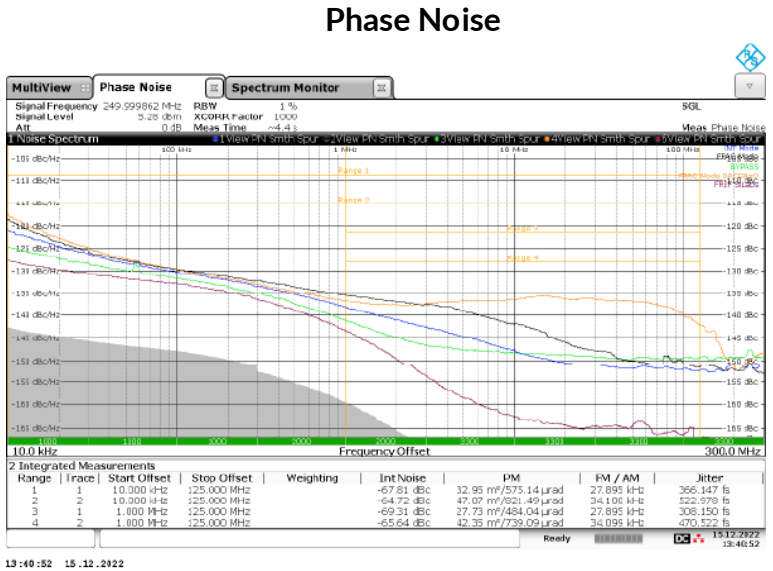
- Low supply noise of clock tree (+PDN impedance)
- Short output clock path
- Period-jitter optimized output IO
- Low noise VDDIO=VDDHV analog supply
- ↗ FREF(FPFD) ↘jitter
- ↗FVCO ↘jitter
- Jitter-optimized XO, GPIO or differential Rx
- Frequency stability of FREF source (e.g. crystal)

Importance depends on the target jitter specs. Consult your IP vendor.

Types of Jitter : Long-Term Jitter (TIE)



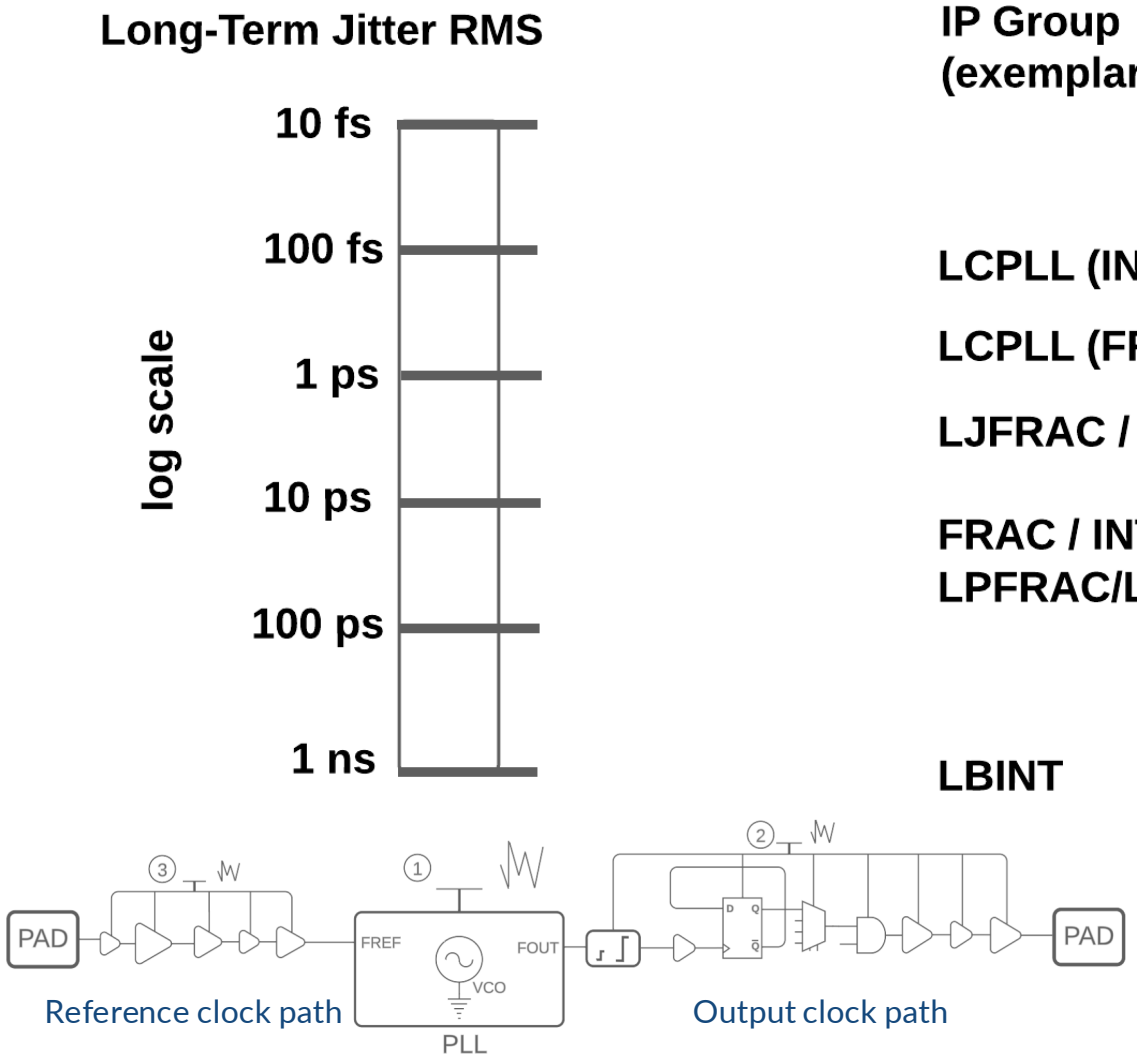




Long Term Jitter

- Long Term Jitter is the deviation of the output phase from the ideal. Output phase is the sum of all period errors.
- Primary concern for ADC/DAC, RF, SERDES.
- LTJ can be natively measured by oscilloscope or by integrating phase noise over certain frequency bands.
- Jitter can be decomposed into random and spurious components.

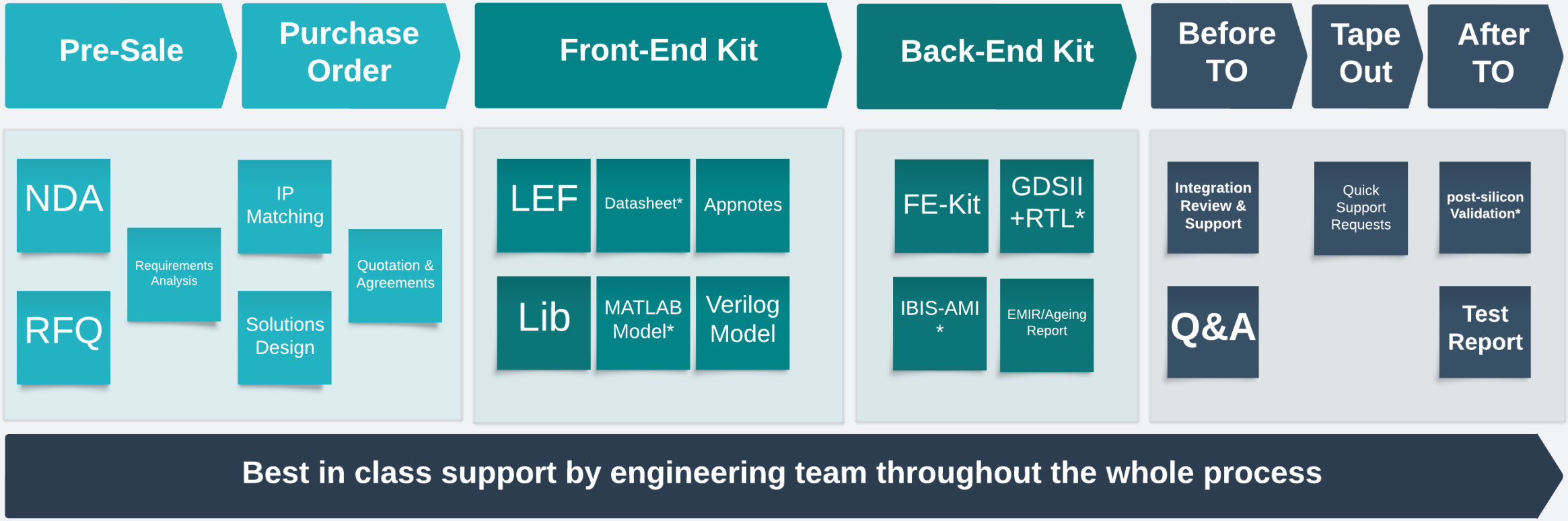
Long-Term Jitter (TIE) & System Contributions



Important design aspects for best performance

- ↗ FREF(FPFD) ↘jitter – allows for higher PLL BW
- ↗FVCO ↘jitter
- Low noise VDDIO=VDDHV analog supply
- Low phase-noise FREF source (e.g., High-quality XO, Clocking Chip)
- Phase Jitter-optimized XO, GPIO or differential Rx
- Phase-Jitter optimized GPIO or differential Tx as test point

IP Engagement Process



- **Silicon Creations engineering team is involved from the beginning to help design SoC clock systems, from IP through distribution to the power delivery network.**

- Stringent performance requirements for the clocking systems (**ultra-low jitter**, **low power**, **wide tuning range**, and **small form factor**) mandate careful IP selection, design considerations, and optimization tradeoffs.

- Silicon Creations clocking/IO/XO IP portfolio **is diversified and well-positioned** to meet the demands of today's SoCs from **2nm** up to 180nm.

- Best-quality IP with experienced support engineers are the key to first silicon success.

- Please reach out to us with any questions or comments: support@siliconcr.com