About Silicon Creations

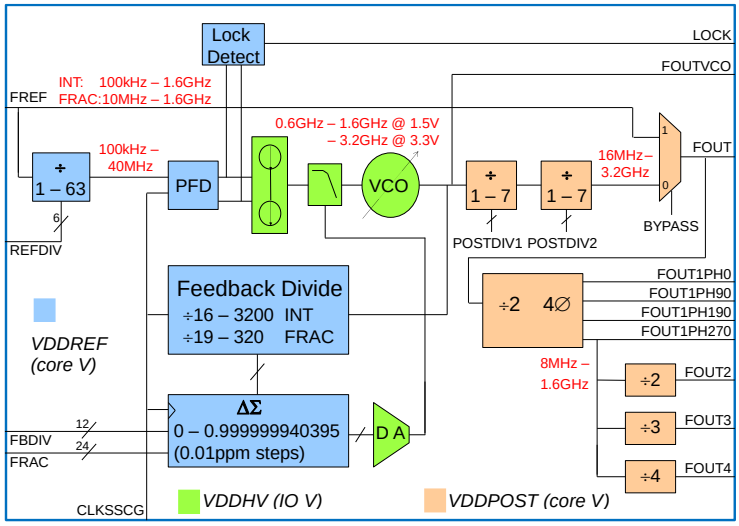
Silicon Creations is focused on providing world-class silicon intellectual property (IP) for precision and general-purpose timing (PLLs), SerDes and high-speed differential I/Os. Silicon Creations' IP is in development in 5nm and is in production from 7nm to 180nm for diverse applications including smart phones, wearables, consumer devices, processors, network devices and medical devices.

With a complete commitment to customer success, Silicon Creations' IP has an excellent record of first silicon to mass production in over 350 chips for over 150 customers and has earned "best-of" awards from TSMC and SMIC.

Silicon Creations, founded in 2006, is self-funded and growing. The company has development centers in Atlanta, USA, and Krakow, Poland, and worldwide sales representation.

General Purpose Fractional-N Ring PLLs

- ✓ Comprehensive programmability and very wide range so suitable for most applications
- ✓ Best power/area/performance tradeoff of any PLL IP – jitter below 2ps RMS in FRAC mode or power below 1mW possible
- ✓ Great supply rejection, no injection locking, zero keep-out and allows shared supplies
- ✓ Digital modulation provides an exact SSCG
- ✓ In mass production from 180nm to 7nm, developing 5nm



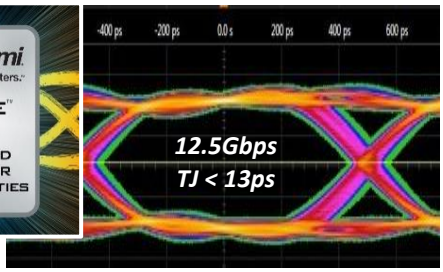
Other Ring PLL IP

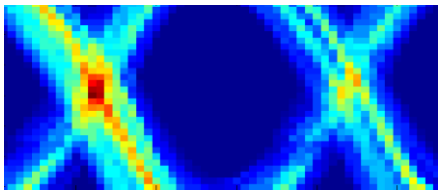
Our flexible self-biased architecture and silicon verified and repeatable jitter/power/area optimization tools allow us to quickly create application-optimized PLLs. Silicon proven examples include:

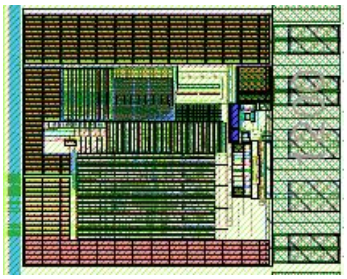
PLL Type	Key feature	Example applications
Jitter optimized integer PLLs	Integer LT Jitter < 0.8ps RMS	Clocking high-end ADCs, DACs and AFEs, SerDes reference clock
Tiny, low power ring PLLs	Area = 0.012mm^2 (40nm), core Vdd only	Digital clocking
Power-optimized ring PLLs	Power < 5µW	Low power clocks for CODECs and battery-operated devices
Low bandwidth & IoT PLLs	Fref = 32kHz watch Xtal, output usable in < 40 cycles	Very low system power clocks for mobile audio and IoT devices
Digital loop filter for Fractional-N PLL	Bandwidth < 50Hz and output long term jitter < 1ps RMS	Clock de-spreading and Jitter attenuation

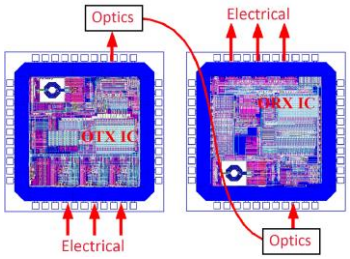
SerDes

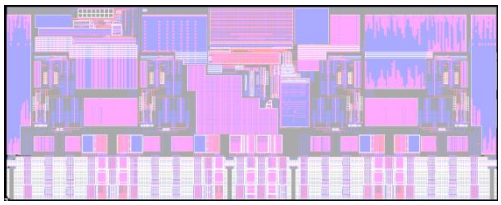
- ✓ One CDR architecture proven from 180nm to 28nm and from <100Mbps to 20Gbps
- ✓ Wide range: over 10:1 data rate from one IP
- ✓ Integrated jitter below 0.7ps RMS from a crystal reference clock
- ✓ Custom, semi-custom and standards-based interfaces available including V-by-One HS, XAUI, SATA, JESD204B, OIF-CEI, CPRI, SGMII, 10G-KR and Multiprotocol to 12.7Gbps





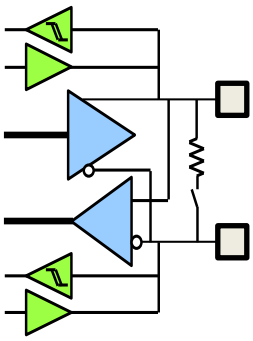






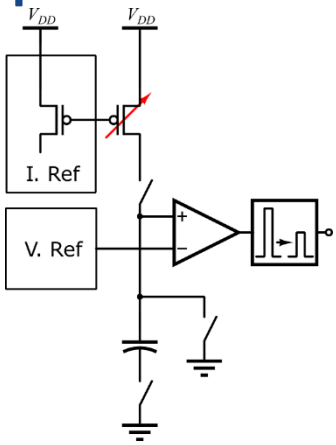
LVDS-based Interfaces

- ✓ Custom, semi-custom and standards-based interfaces available including FPD Link, FastLVDS, OpenOLDI, CameraLink, Mini LVDS
- ✓ Robust and wide range: dynamic phase alignment and pixel clocks from <10MHz to >200MHz; line rates over 3Gbps



Free Running Oscillators

- ✓ Power below 30µW possible
- ✓ Accuracy over PVT after trimming better than ±1.5% possible
- ✓ 7nm to 65nm



Processes Supported

- ✓ Silicon Creations IP is TSMC IP 9000 qualified and is proven or in mass production in many processes
- ✓ Automotive/ISO26262 safety supported
- ✓ Our in-house PDKs and standard cells mean our IP does not require third party licenses and we can port our IP to new processes very quickly and with low risk

tsmc UMC TOWERJAZZ IBM TOSHIBA Leading Innovation SMIC SAMSUNG Dongbu HiTek RENESAS GLOBALFOUNDRIES

Fin Fet: 7nm, 8/10nm, 12/16nm; FDSOI: 22nm, 28nm
CMOS: 22/28nm, 40/45nm, 55/65nm, 90nm, 130nm, 180nm

Contact Us

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