Silicon Creations Celebrates 100th Tape-Out of Its PLL in TSMC 28nm Process Technology

SUWANEE, Ga., September 11, 2017 — Silicon Creations today announced its general-purpose fractional phase-locked loop (PLL) IP has surpassed 100 mass production tape-outs on TSMC's 28nm process node.

Silicon Creations, a leading supplier of high-performance analog and mixed-signal intellectual property (IP), had its first tape-out of its high-performance 24-bit Fractional-N PLL in TSMC 28nm (PLLTS28HPMFRAC) in 2011, but more than half of the production releases of chips using this PLL have been in the last 18 months, stated Randy Caplan, co-founder of Silicon Creations.

The 28nm node has hit a chord for customers, he noted. More than 600,000 wafers have been produced using the PLLTS28HPMFRAC for over 25 unique customers, Silicon Creations' highest volume on a TSMC process. Silicon Creations continues to push its technology into smaller nodes with production in more than 20 chips at TSMC's 16nm and10nm nodes and proven PLLs in 7nm.

"TSMC's extremely accurate models provide predictable silicon results, and they have industry-leading process control, which gives us high yield," continued Caplan. "TSMC's process technology reduces time to market and risk, and is easy to integrate."

TSMC's 28HPC (28-nanometer High Performance Compact) was launched in 2014 for volume production as the most power- and cost-efficient solution among all 28-nanometer technologies in the foundry segment. As a compact version of TSMC's 28HPM, 28HPC is optimized for customers' architectures to realize competitive die size and product performance for the new generation of cost-effective mobile and consumer devices, delivering a highly competitive performance/cost advantage. In 2015 TSMC launched the enhanced version of this same process, 28HPC+, with even more compact libraries and improved performance.

“Thanks to innovative design, Silicon Creations has been able to support all variants of TSMC’s 28nm metal gate processes with a single layout of the PLLTS28HPMFRAC,” Caplan said. “This has led to many benefits for our customers including lowered risk, raised yield and shorter time to market.”

Caplan added that the PLL’s wide programmability has allowed customers to use multiple instances of the PLL to generate clocks with widely different requirements, ranging from a PCIe3 reference to spread spectrum references for LPDDR interfaces. In fact, one customer has a chip in production using 17 instances of the PLL, many of which are able to share power supplies which have saved package pins, he said.

As a TSMC IP Alliance member, Silicon Creations’ extensive portfolio of PLL and high-speed I/O IPs has been qualified through the TSMC IP9000 program for a number of processes ranging from 180nm to 10nm. These IPs, along with the TSMC 40nm LP SerDes PMA, will be showcased at the upcoming TSMC OIP Ecosystem Forum on September 13, 2017 held at the Santa Clara Convention Center in Santa Clara, California.

About

Silicon Creations is focused on providing world-class silicon intellectual property (IP) for precision and general-purpose timing (PLLs), SerDes and high-speed differential I/Os. Silicon Creations’ IP is proven from 7- to 180-nanometer process technologies. With a complete commitment to customer success, its IP has an excellent record of first silicon to mass production in customer designs. Silicon Creations, founded in 2006, is self-funded and growing. The company has development centers in Atlanta, Ga., and Krakow, Poland, and worldwide sales representation. For more information, visit www.siliconcr.com.

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