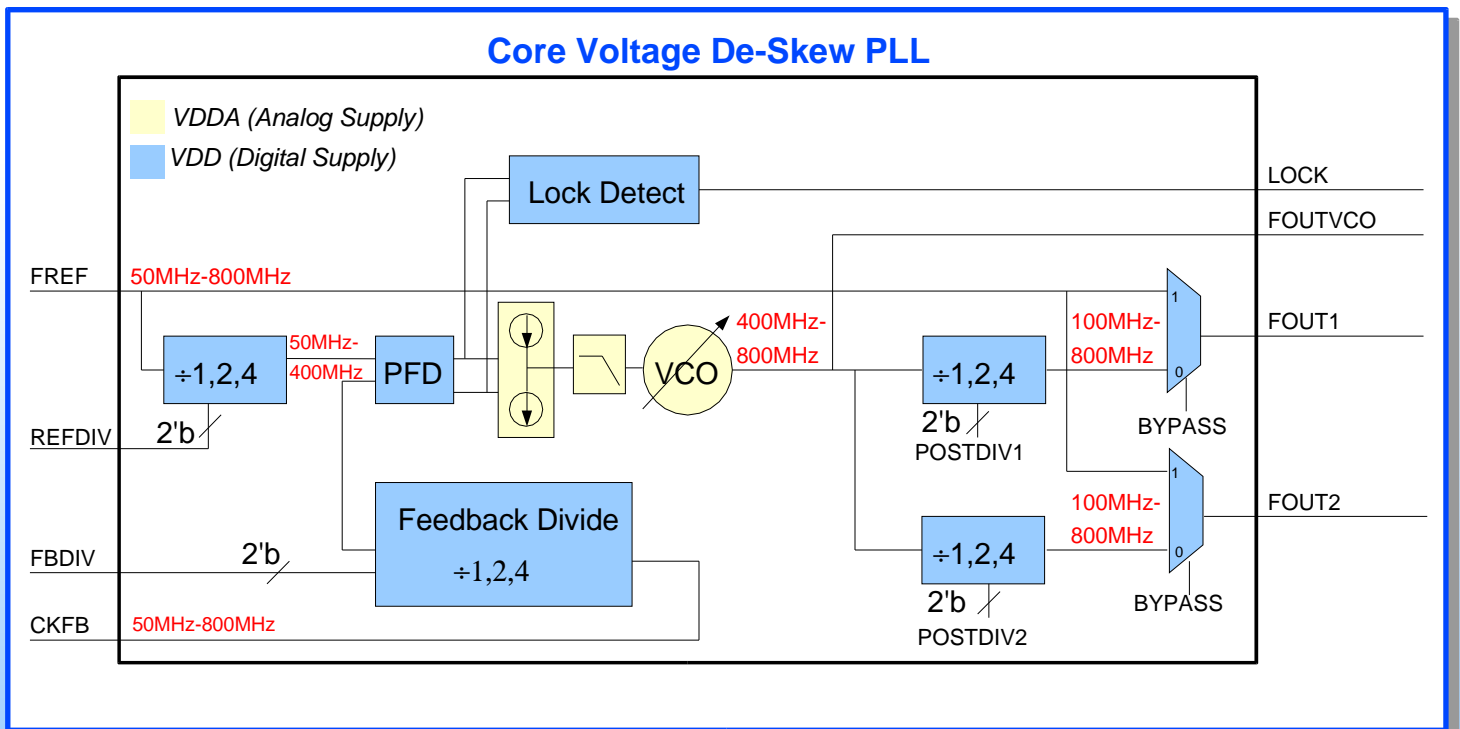


Overview

The Silicon Creations Programmable De-Skew PLL is a high bandwidth, low jitter design optimized to minimize phase skew at its inputs. Wide input and output ranges along with best-in-class jitter performance allow the PLL to be used for almost any de-skew application. With excellent supply noise immunity, the PLL is ideal for use in noisy mixed signal SoC environments. By combining ultra-low jitter output clocks into a low power, low area, widely programmable design, Silicon Creations can reduce risk and time-to-market by enabling a single macro to be used for any clock de-skewing application.

Features

- Input Frequency Range: 50MHz to 800MHz
- Feedback Frequency Range: 50MHz to 800MHz
- Output Frequency Range: 100MHz to 800MHz
- Static Phase Error (max, 6-sigma): +50ps
- Input-Output Jitter: <5ps RMS (FREF=400MHz)
- 2:1 VCO frequency range
- Core Voltage analog supply
- Lock Detect Signal indicates when frequency lock has been achieved
- Low Area (0.04mm²)



Maximum Operating Conditions

	Condition	Minimum	Typical	Maximum
V _{DDA}	Analog Supply Voltage	1.08V	1.2V	1.32V
V _{DD}	Digital Supply Voltage	1.08V	1.2V	1.32V
T _J	Junction Temperature	-40°C	25°C	125°C

PLL Specifications

Parameter	Units	Min	Typ	Max	Comment
VDDA Current Consumption (F _{VCO} = 800MHz)	mA		2	2.4	Current scales as (F _{VCO} /800MHz) ^{1.5} Example: For F _{VCO} = 400MHz, Current = (400MHz/800MHz) ^{1.5} * 2mA = 708µA
VDD Power Consumption (1.2V)	µW/MHz		2	2.4	Specification is based on VCO frequency. VDD=1.2V. Power scales as VDD ² .
Power Down Leakage	µA		1		Temp = 27C
Reference Range	MHz	50		800	Divided reference clock (FREF/REFDIV) should be 400MHz maximum
Output Range	MHz	100		800	
Feedback Range	MHz	50		800	
Feedback Path Delay	Ref Clock Cycles			1.5	Input Clock cycle is REFDIV/FREF.
Output Duty Cycle	%	47.5	50	52.5	@800MHz (falling edge error is +31ps)
Static Phase Error	ps	-50		50	6-sigma, peak
Lock Time	Ref Clock Cycles		4000	8000	Ref Clock cycle is REFDIV/FREF. Example: FREF=400MHz, REFDIV=1, Lock time = 10µs
Period Jitter (Random)	ps (RMS)			1	@1GHz. Random jitter scales as SQRT(1GHz/FOUT)
Cycle Jitter (Random)	ps (RMS)			1.5	
Period Jitter Supply Noise Sensitivity	ps/mV (p-p)		0.2		This value depends heavily on the relationship between FOUT and the frequency content of the VDD noise. Please contact Silicon Creations (support@siliconcr.com) for a detailed analysis of a specific setting.
Cycle -Cycle Jitter Supply Noise Sensitivity	ps/mV (p-p)		0.3		
Long Term (Input to Output) Jitter	ps RMS			5	Random contribution only. Fref=400MHz. Total LTJ is approximately this value plus the period jitter induced by supply noise
Area	mm ²		0.04		200µm x 200µm
Process		1P4M	1.2V/3.3V		Compatible with all metal options 4M and above. No additional masks required.

Silicon Creations

49 Highway 23 NE
Suwanee, GA 30024
www.siliconcr.com

Tel: (866) 232-3431
Fax: (678) 259-9301
sales@siliconcr.com