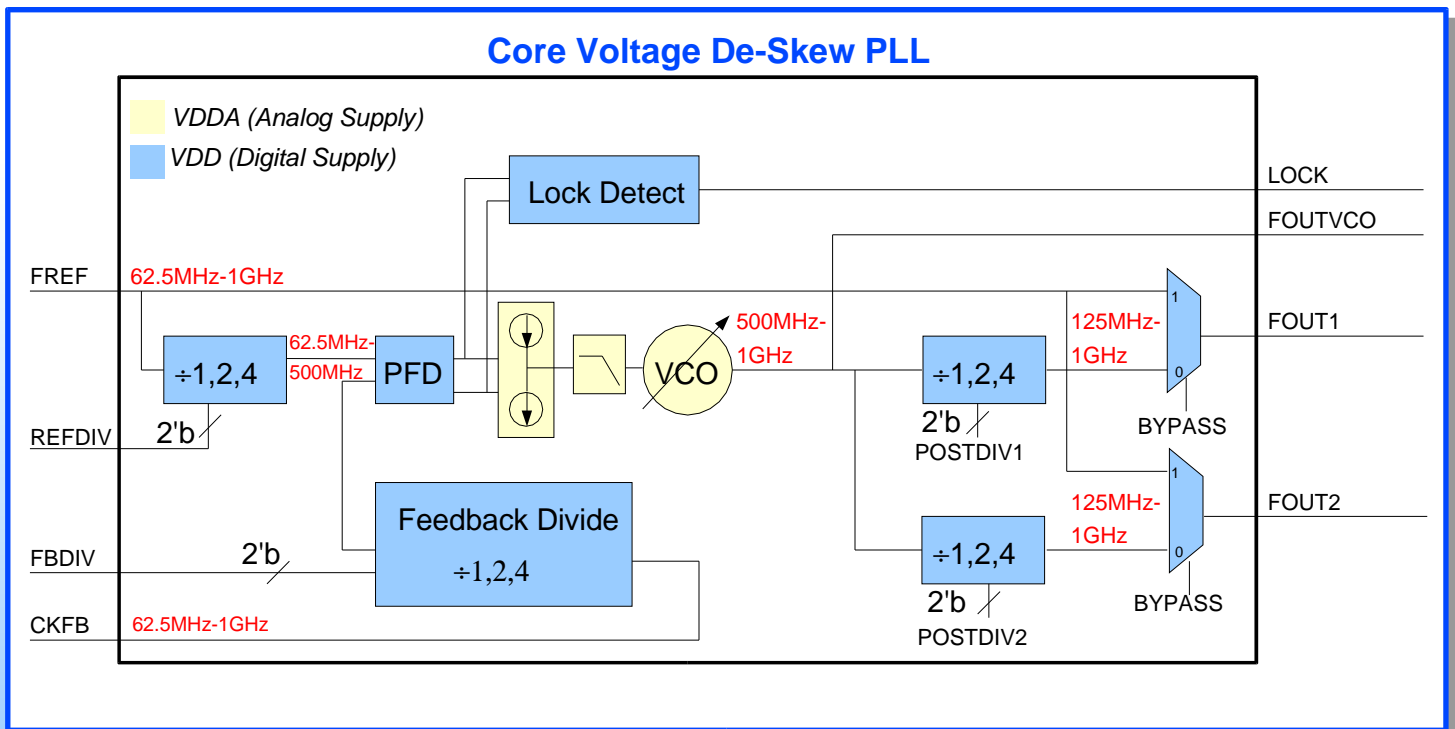


Overview

The Silicon Creations Programmable De-Skew PLL is a high bandwidth, low jitter design optimized to minimize phase skew at its inputs. Wide input and output ranges along with best-in-class jitter performance allow the PLL to be used for almost any de-skew application. With excellent supply noise immunity, the PLL is ideal for use in noisy mixed signal SoC environments. By combining ultra-low jitter output clocks into a low power, low area, widely programmable design, Silicon Creations can reduce risk and time-to-market by enabling a single macro to be used for any clock de-skewing application.

Features

- Input Frequency Range: 62.5MHz to 1GHz
- Feedback Frequency Range: 62.5MHz to 1GHz
- Output Frequency Range: 125MHz to 1GHz
- Static Phase Error (max, 6-sigma): +50ps
- Input-Output Jitter: <5ps RMS (FREF=500MHz)
- 2:1 VCO frequency range
- Core Voltage analog supply
- Lock Detect Signal indicates when frequency lock has been achieved
- Low Area (0.04mm²)



Maximum Operating Conditions

	Condition	Minimum	Typical	Maximum
V _{DDA}	Analog Supply Voltage	0.9V	1.0V or 1.2V (OD)	1.32V (OD)
V _{DD}	Digital Supply Voltage	0.9V	1.0V or 1.2V (OD)	1.32V (OD)
T _J	Junction Temperature	-40°C	25°C	125°C

PLL Specifications

Parameter	Units	Min	Typ	Max	Comment
VDDA Current Consumption (F _{VCO} = 1GHz)	mA		2	2.4	Current scales as (F _{VCO} /1GHz) ^{1.5} Example: For F _{VCO} = 500MHz, Current = (500MHz/1GHz) ^{1.5} * 2mA = 708μA
VDD Power Consumption (1.0V)	μW/MHz		2	2.4	Specification is based on VCO frequency. VDD=1.0V. Power scales as VDD ² .
Power Down Leakage	μA		10		Temp = 27C
Reference Range	MHz	62.5		1000	Divided reference clock (FREF/REFDIV) should be 400MHz maximum
Output Range	MHz	125		1000	
Feedback Range	MHz	62.5		1000	
Feedback Path Delay	Ref Clock Cycles			1.5	Input Clock cycle is REFDIV/FREF.
Output Duty Cycle	%	47.5	50	52.5	@1GHz (falling edge error is +-25ps)
Static Phase Error	ps	-50		50	6-sigma, peak
Lock Time	Input clock cycles		4000	8000	Input Clock cycle is REFDIV/FREF. Example: FREF=500MHz, REFDIV=1, Lock time = 8μs
Period Jitter (Random)	ps (RMS)			1	@1GHz. Random jitter scales as SQRT(1GHz/FOUT)
Cycle Jitter (Random)	ps (RMS)			1.5	
Period Jitter Supply Noise Sensitivity	ps/mV (p-p)		0.2		This value depends heavily on the relationship between FOUT and the frequency content of the VDD noise. Please contact Silicon Creations (support@siliconcr.com) for a detailed analysis of a specific setting.
Cycle -Cycle Jitter Supply Noise Sensitivity	ps/mV (p-p)		0.3		
Long Term (Input to Output) Jitter	ps RMS			5	Random contribution only. Fref=500MHz. Total LTJ is approximately this value plus the period jitter induced by supply noise
Area	mm ²		0.04		200μm x 200μm
Process		1P4M	1.0V/2.5V		Compatible with all metal options 4M and above. No additional masks required.

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