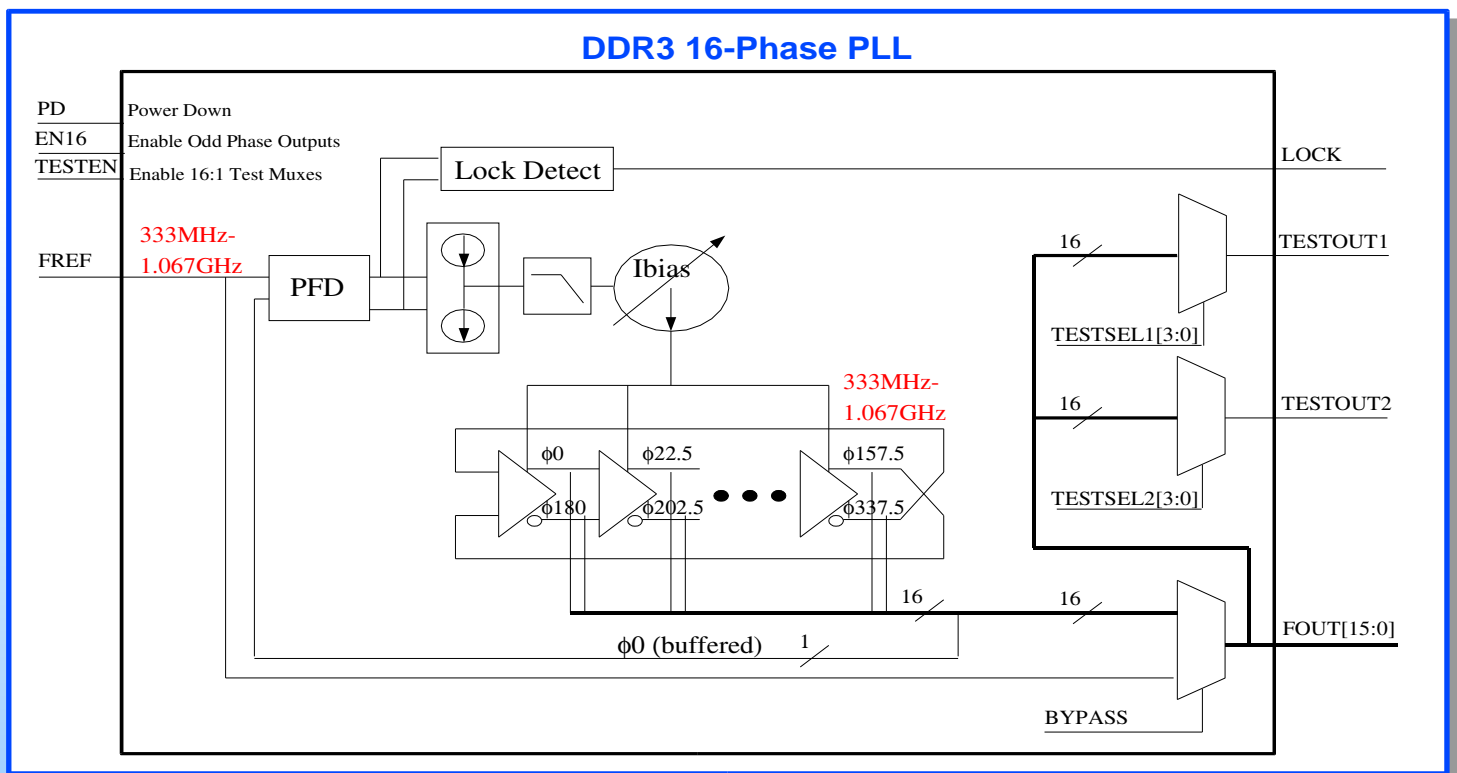


Overview

The Silicon Creations DDR3 High Bandwidth PLL is designed to accurately generate 16 clocks with equally spaced phases, and frequency equal to the input reference clock. With a nominal loop bandwidth of $F_{REF}/100$, the PLL can quickly track any frequency variations in the input clock while simultaneously filtering any rapid phase changes (i.e. short-term jitter). Additionally, excellent supply noise immunity makes the PLL well suited for use in noisy mixed signal SoC environments.

Features

- Input Frequency Range: 333MHz to 1.067GHz
- Output Frequency Range: 333MHz to 1.067GHz
- 16 output clocks with equally spaced phases
- Option to disable every-other phase to save power in 8-phase operation
- Two test output muxes allow any of the 16 phases to be observed individually
- 3:1 VCO frequency range allows PLL to cover the full input/output range without any coarse steps or digital adjustment
- Proprietary PLL core architecture allows for excellent supply rejection in noisy SoC applications
- Lock Detect Signal indicates when frequency lock has been achieved
- Low Area (0.027mm^2)



Maximum Operating Conditions

	Condition	Minimum	Typical	Maximum
V _{DD}	Supply Voltage	0.81V	0.9V	1.1V (OD)
T _J	Junction Temperature	-40°C	25°C	125°C

PLL Pin List

Pin Name	# of Bits	Type	Function	Notes / Restrictions
FREF	1	Input	Reference Clock	333MHz-1.067GHz
PD	1	Input	Global Power Down	Active High
EN16	1	Input	16-Phase Operation Enable	Odd phases are powered down when EN16 equals 0
TESTEN	1	Input	Test Mux Enable	Enables test mux
TESTSEL1	4	Input	Select Phase for Mux 1	Selects FOUT phase example: 4'b0000= FOUT[0] 4'b1111 = FOUT[15]
TESTSEL2	4		Select Phase for Mux 2	
BYPASS	1	Input	Bypass PLL	FOUT[15:0] = FREF
TESTOUT1	1	Output	Test Mux Output 1	Test clock Output (FOUT or FREF)
TESTOUT2	1	Output	Test Mux Output 2	Test clock Output (FOUT or FREF)
FOUT	16	Output	16-Phase Output Clocks	Frequency = FREF Phase ° = 22.5 * N (for FOUT[N])
LOCK	1	Output	PLL Lock Signal	Implies no cycles slips in 512 consecutive reference cycles

PLL Specifications

Parameter	Units	Min	Typ	Max	Comment
VDD Power Consumption (0.9V)	μW/MHz		7	9	Power scales as VDD ² .
Power Down Leakage	μA		100		Temp = 27C
Input / Output Freq. Range	MHz	333		1067	
Output Duty Cycle	%	48	50	52	@1GHz (falling edge error is +-20ps)
Lock Time	μs		5	10	
Phase-Phase Variation	% Period	-1.8		1.8	1.067GHz (p-p, 6σ)
Phase-Phase Variation	% Period	-3		3	333MHz (p-p, 6σ)
Period Jitter (p-p, 6σ)	% Period	-1.5		1.5	Assumes a maximum of 10% peak-to-peak supply noise (VDD-VSS).
Long Term Jitter (p-p, 6σ)	% Period	-3		3	
Area	mm ²		0.03		200μm x 135μm
Process		1P4M	0.9V/2.5V		Compatible with all metal options 4M and above. No additional masks required.

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