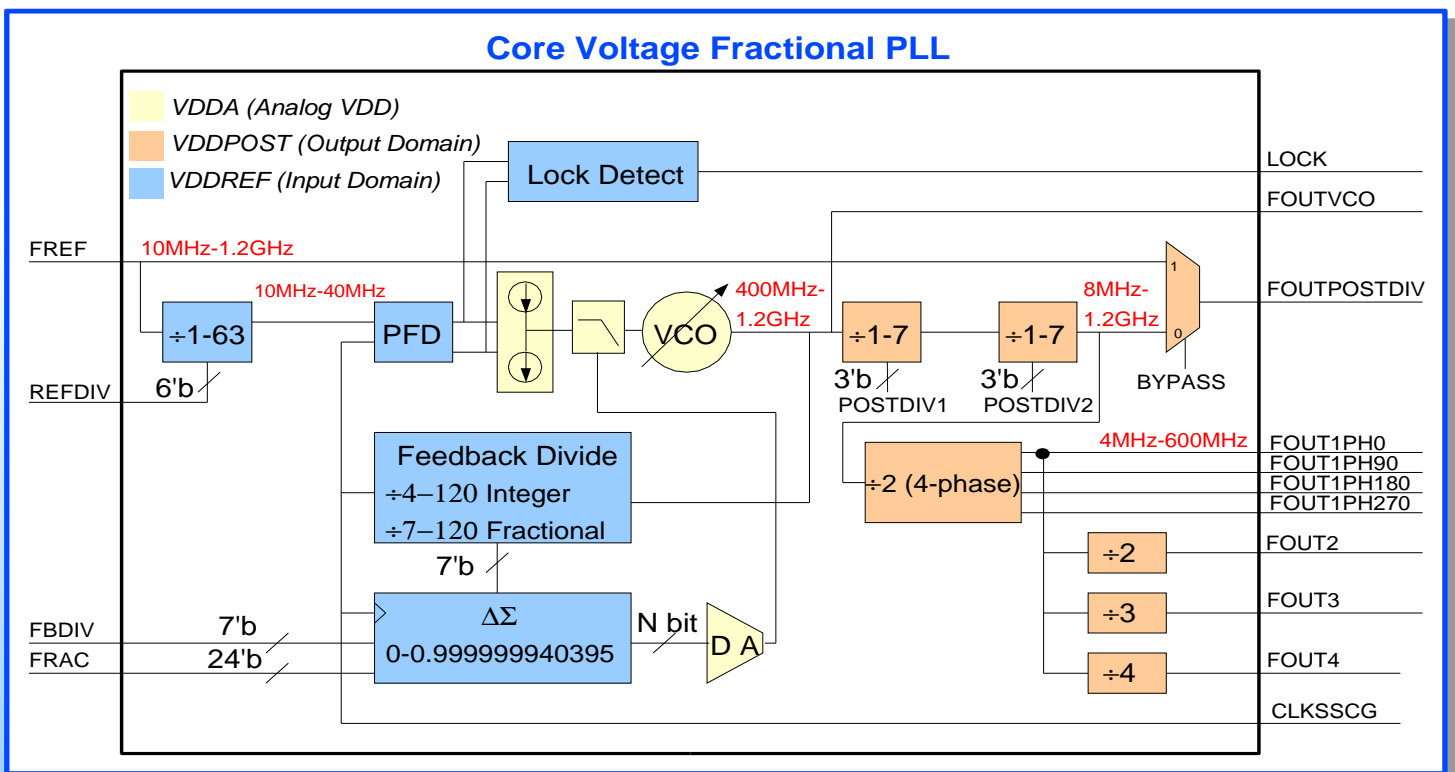


Overview

The Silicon Creations Programmable Delta Sigma Fractional PLL is a multi-function, general purpose frequency synthesizer. Ultra-wide input and output ranges along with best-in-class jitter performance allow the PLL to be used for almost any clocking application. With excellent supply noise immunity, the PLL is ideal for use in noisy mixed signal SoC environments. By combining ultra-low jitter output clocks into a low power, low area, widely programmable design, Silicon Creations can greatly simplify an SoC by enabling a single macro to be used for all clocking applications in the system.

Features

- Input Frequency Range: 10MHz to 1.2GHz
- Output Frequency Range: 1MHz to 1.2GHz
- 24 bit fractional accuracy
 - $\Delta\Sigma$ noise cancellation DAC allows fractional mode jitter performance to nearly match integer mode performance
- 3:1 VCO frequency range allows PLL to be optimized for minimum jitter or minimum power
- Operates off of a single core voltage supply
- Lock Detect Signal indicates when frequency lock has been achieved
- Low Area (0.07mm²)



Maximum Operating Conditions

	Condition	Minimum	Typical	Maximum
V _{DDA}	Analog Supply Voltage	0.81V	0.9V	0.99V
V _{DDREF} / V _{DDPOST}	Digital Supply Voltage	0.81V	0.9V	0.99V
T _J	Junction Temperature	-40°C	25°C	125°C

PLL Specifications

Parameter	Units	Min	Typ	Max	Comment
VDDA Current Consumption (F _{VCO} = 1GHz)	mA		1	1.2	Current scales as (F _{VCO} /1GHz) ^{1.5} Example: For F _{VCO} = 600MHz, Current = (600MHz/1GHz) ^{1.5} * 1mA = 464μA
VDD Power Consumption (0.9V) (VDDREF+VDDPOST)	μW/MHz		3	4	Specification is based on VCO frequency. VDD=0.9V. Assumes all features are enabled, so power should be lower for most applications. Power scales as VDD ² .
Power Down Leakage	μA		100		Temp = 27C
Reference Frequency Range	MHz	10		1200	Divided reference clock (FREF/REFDIV) should be 40MHz maximum
VCO Frequency Range	MHz	400		1200	Maximum VCO frequency depends on nominal supply voltage (see "VCO Frequency Table" in block diagram above)
Output Frequency Range	MHz	1		1200	
Output Duty Cycle	%	45	50	55	@1GHz (falling edge error is +50ps)
Lock Time	μs			40	Output frequency is within 0.1% of target
Period Jitter (p-p, 6σ)	% Output Period	-2		2	Assumes a maximum of 10% peak-peak supply noise (VDDPOST – VSS)
Cycle - Cycle Jitter (p-p, 6σ)	% Output Period	-3		3	Assumes a maximum of 10% peak-peak supply noise (VDDPOST – VSS)
Long Term Jitter (Integer mode)	ps RMS			12	Fref = 27MHz, FVCO=1GHz Note: Long term jitter improves with higher FREF and higher FVCO
Long Term Jitter (Fractional mode)	ps RMS			20	Fref = 27MHz, FVCO=1GHz
Area	mm ²		0.07		200μm x 350μm
Process		1P4M	0.9V/2.5V		Compatible with all metal options 4M and above. No additional masks required.

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