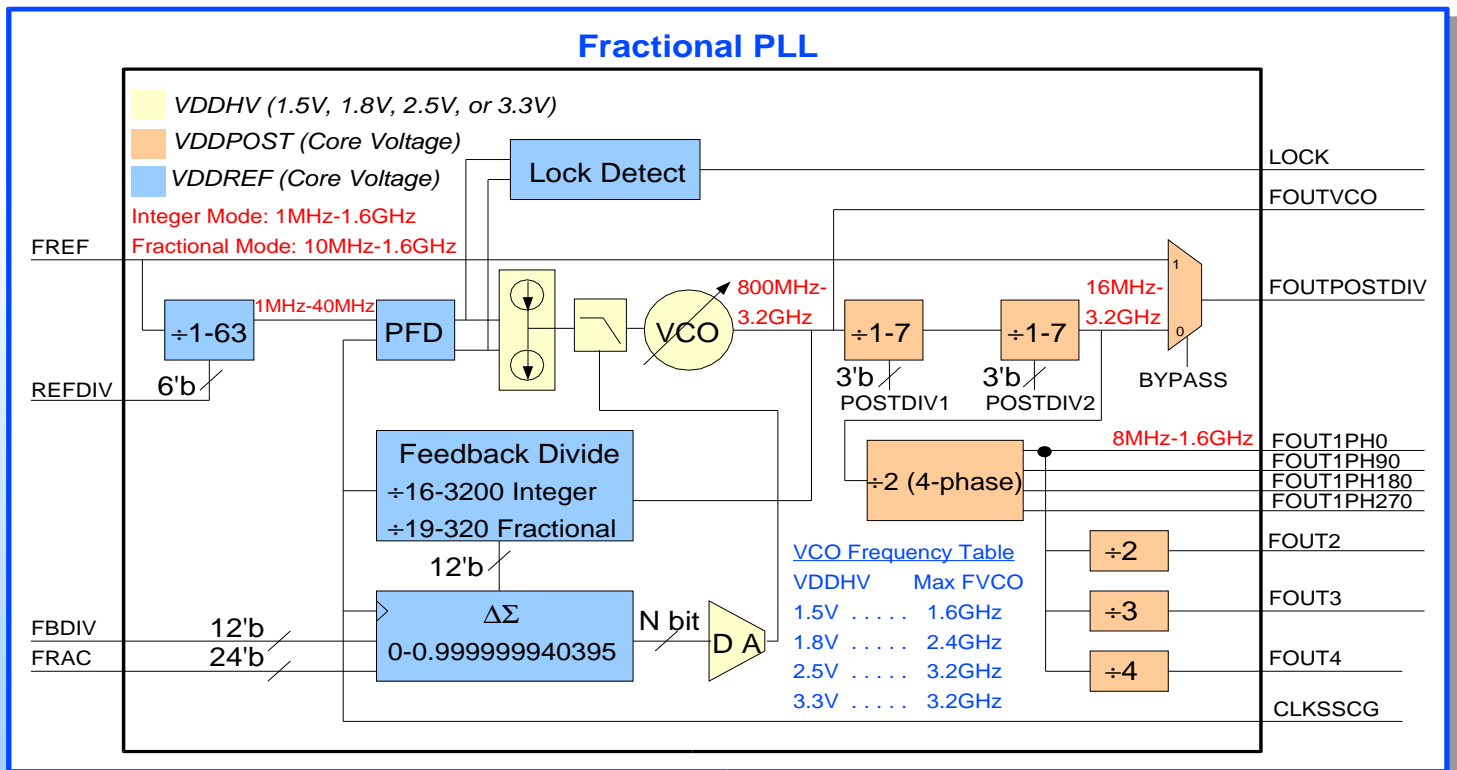


## Overview

The Silicon Creations Programmable Delta Sigma Fractional PLL is a multi-function, general purpose frequency synthesizer. Ultra-wide input and output ranges along with best-in-class jitter performance allow the PLL to be used for almost any clocking application. With excellent supply noise immunity, the PLL is ideal for use in noisy mixed signal SoC environments. By combining ultra-low jitter output clocks into a low power, low area, widely programmable design, Silicon Creations can greatly simplify an SoC by enabling a single macro to be used for all clocking applications in the system.

## Features

- Input Frequency Range: 1MHz to 1.6GHz
  - 10MHz to 1.6GHz (Fractional Mode)
- Output Frequency Range: 2MHz to 3.2GHz
- 24 bit fractional accuracy
  - $\Delta\Sigma$  noise cancellation DAC allows fractional mode jitter performance to nearly match integer mode performance
- 4:1 VCO frequency range allows PLL to be optimized for minimum jitter or minimum power
- Isolated analog supply (1.5V to 3.3V) allows for excellent supply rejection in noisy SoC applications
- Lock Detect Signal indicates when frequency lock has been achieved
- Low Area (0.07mm<sup>2</sup>)



### Maximum Operating Conditions

	Condition	Minimum	Typical	Maximum
V <sub>DDHV</sub>	Analog Supply Voltage	1.35V	1.5V, 1.8V, 2.5V, or 3.3V	3.63V
V <sub>DDREF</sub> , V <sub>DDPOST</sub>	Digital Supply Voltage	0.81V	0.9V	0.99V
T <sub>J</sub>	Junction Temperature	-40°C	25°C	125°C

### PLL Specifications

Parameter	Units	Min	Typ	Max	Comment
VDDHV Current Consumption (F <sub>VCO</sub> = 1GHz)	mA		1	1.2	Current scales as (F <sub>VCO</sub> /1GHz) <sup>1.5</sup> Example: For F <sub>VCO</sub> = 800MHz, Current = (800MHz/1GHz) <sup>1.5</sup> * 1mA = 715µA
VDD Power Consumption (0.9V) (VDDREF+VDDPOST)	µW/MHz		3	4	Specification is based on VCO frequency. VDD=0.9V. Assumes all features are enabled, so power should be lower for most applications. Power scales as VDD <sup>2</sup> .
Power Down Leakage	µA		100		Temp = 27C
Reference Frequency Range	MHz	1		1600	Divided reference clock (FREF/REFDIV) should be 40MHz maximum
VCO Frequency Range	MHz	800		3200	See "VCO Frequency Table" above
Output Frequency Range	MHz	2		3200	Minimum frequency on FOUTPOSTDIV is 16MHz. FOUT4 can output as low as 2MHz.
Output Duty Cycle	%	45	50	55	@1GHz (falling edge error is +50ps)
Lock Time	Input clock cycles		1000	1500	Input Clock cycle is REFDIV/FREF. Example: FREF=27MHz, REFDIV=1, Lock time = 37µs
Period Jitter (Random)	ps (RMS)			1	@1GHz. Random jitter scales as SQRT(1GHz/FOUT)
Cycle Jitter (Random)	ps (RMS)			1.5	
Period Jitter Supply Noise Sensitivity	ps/mV (p-p)		0.2		This value depends heavily on the relationship between FOUT and the frequency content of the VDDPOST noise. Please contact Silicon Creations ( <a href="mailto:support@siliconcr.com">support@siliconcr.com</a> ) for a detailed analysis of a specific setting.
Cycle -Cycle Jitter Supply Noise Sensitivity	ps/mV (p-p)		0.3		
Long Term Jitter (Int)	ps RMS			6	Random contribution only. Fref > 20MHz.
Long Term Jitter (Frac)	ps RMS			10	Total LTJ is approximately this value plus the period jitter induced by supply noise
Area	mm <sup>2</sup>		0.07		200µm x 350µm
Process		1P4M 0.9V/2.5V			Compatible with all metal options 4M and above. No additional masks required.

### Silicon Creations

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